Nanoscale III-V Electronics: InGaAs FinFETs and Vertical Nanowire MOSFETs

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Massachusetts Institute of Technology

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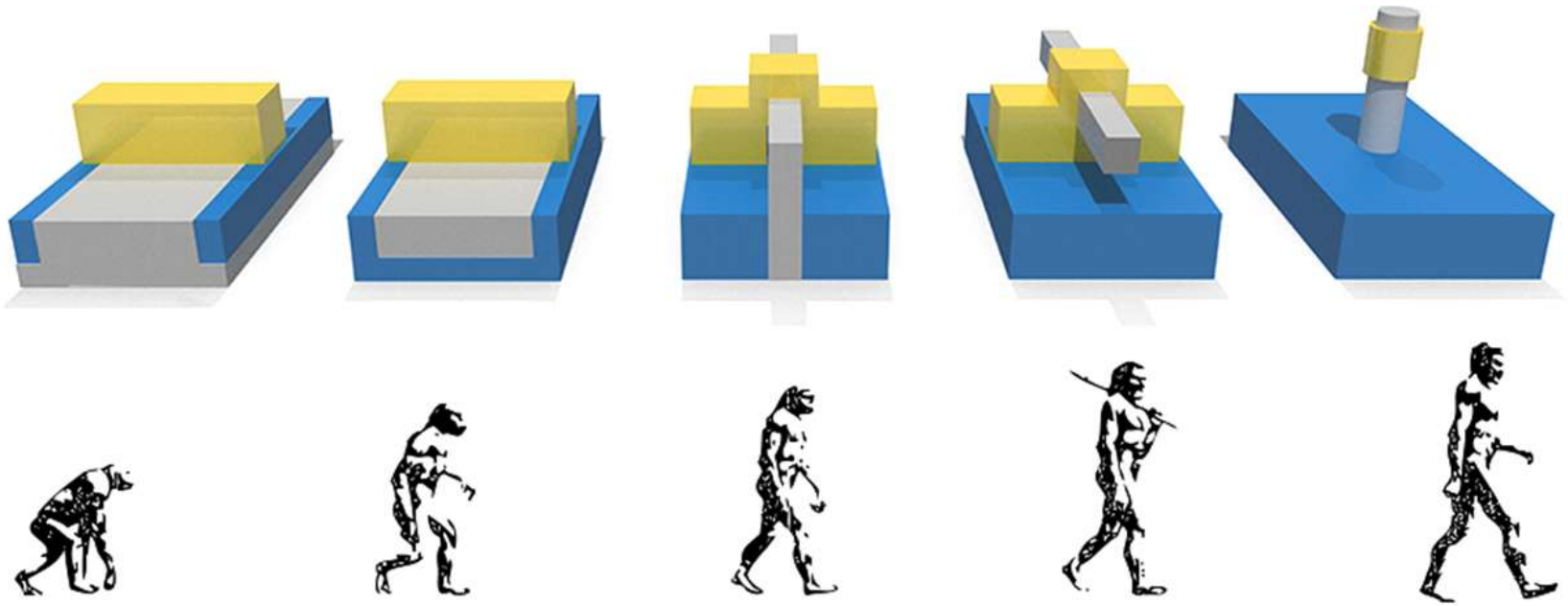
- Labs at MIT: MTL, EBL

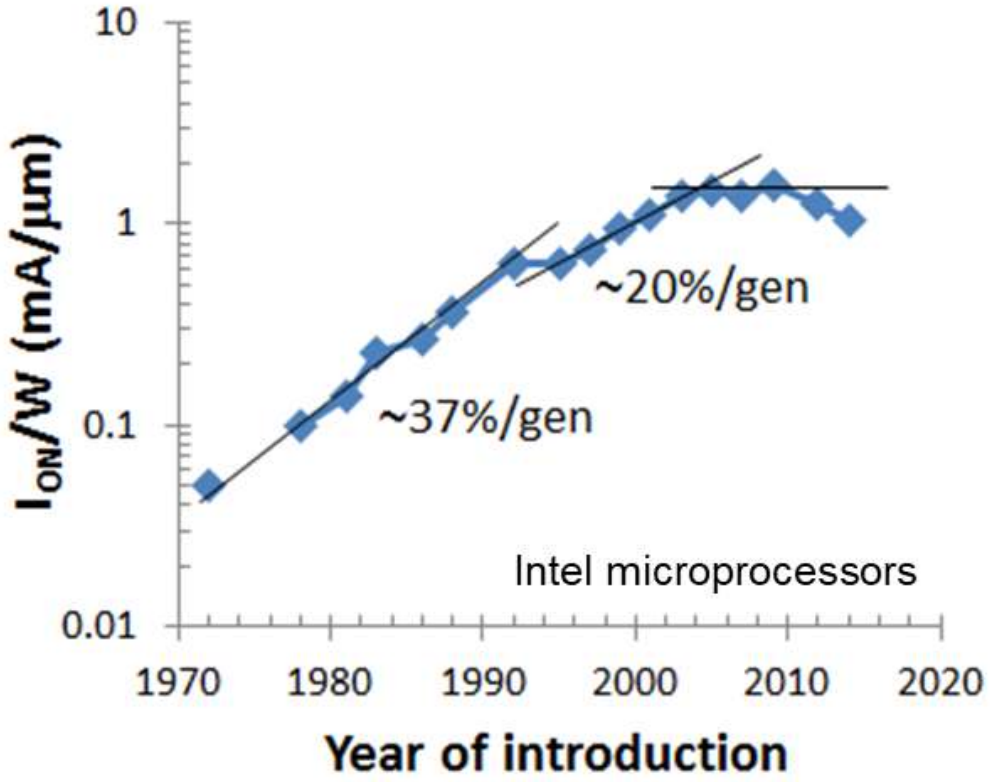
Evolution of transistor structure for improved scalability



Enhanced gate control → improved scalability

Moore's Law: The Problem

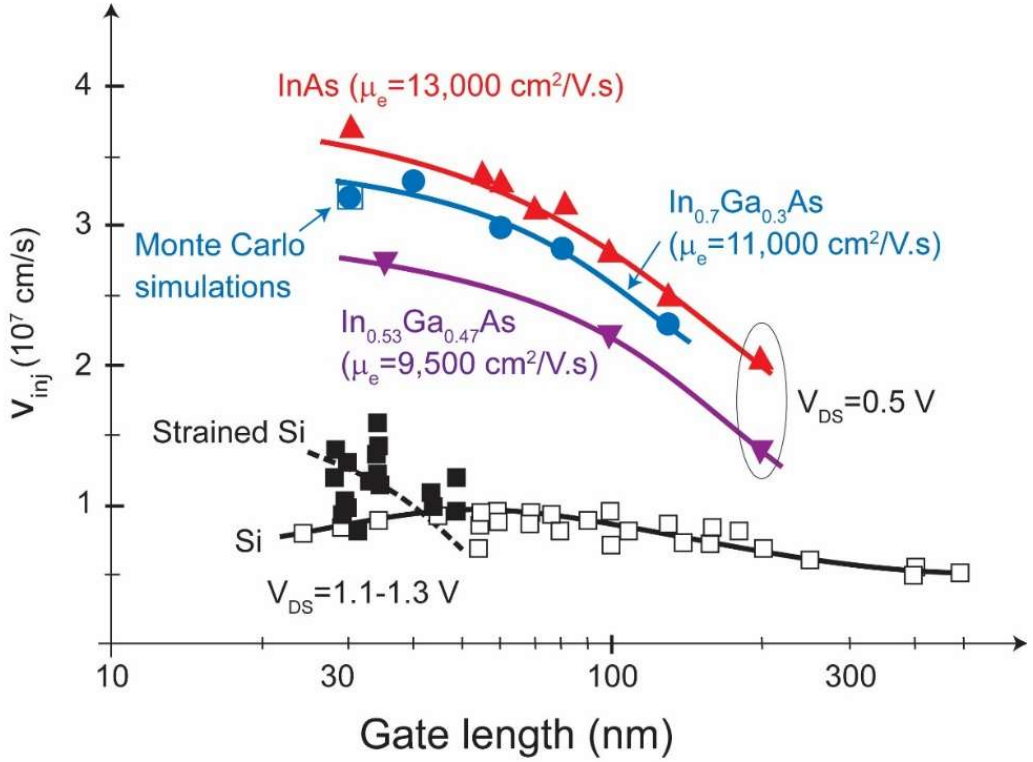
Current density of n-MOSFETs at nominal voltage:



Scaling: Voltage ↓ → Current density ↓ → Performance ↓

III-V CMOS: The Promise

Source injection velocity: Si vs. InGaAs



del Alamo,
Nature 2011

v_{inj}(InGaAs) > 2v_{inj}(Si) at less than half V_{DD}

→ high current at low voltage

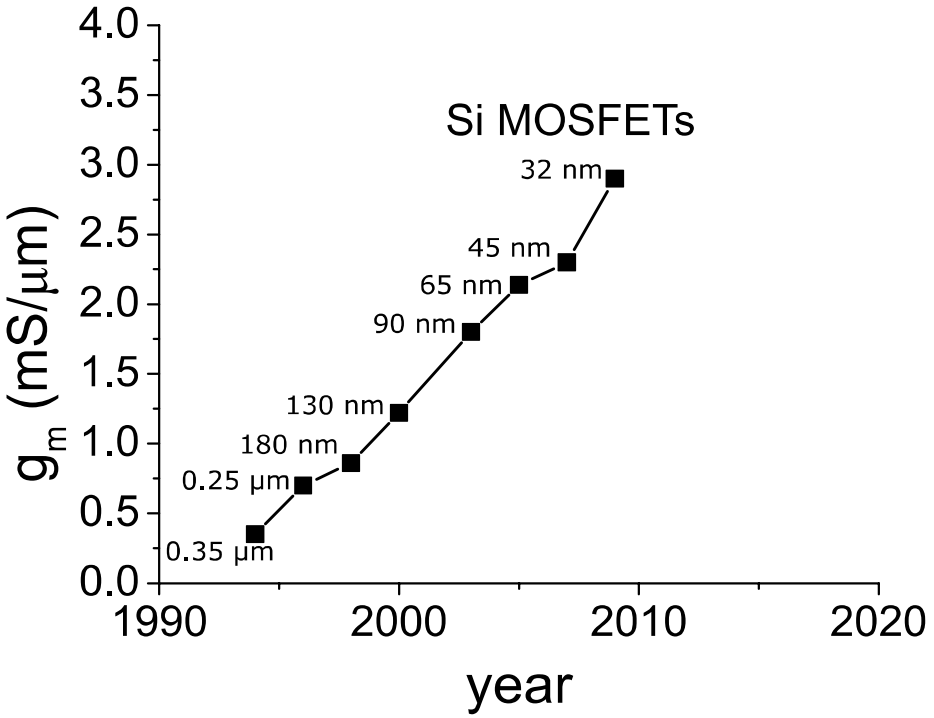
Evolution of transistor structure for improved scalability

Thin-body MOSFET

Enhanced gate control → improved scalability

Transconductance of Planar Si vs. InGaAs MOSFETs

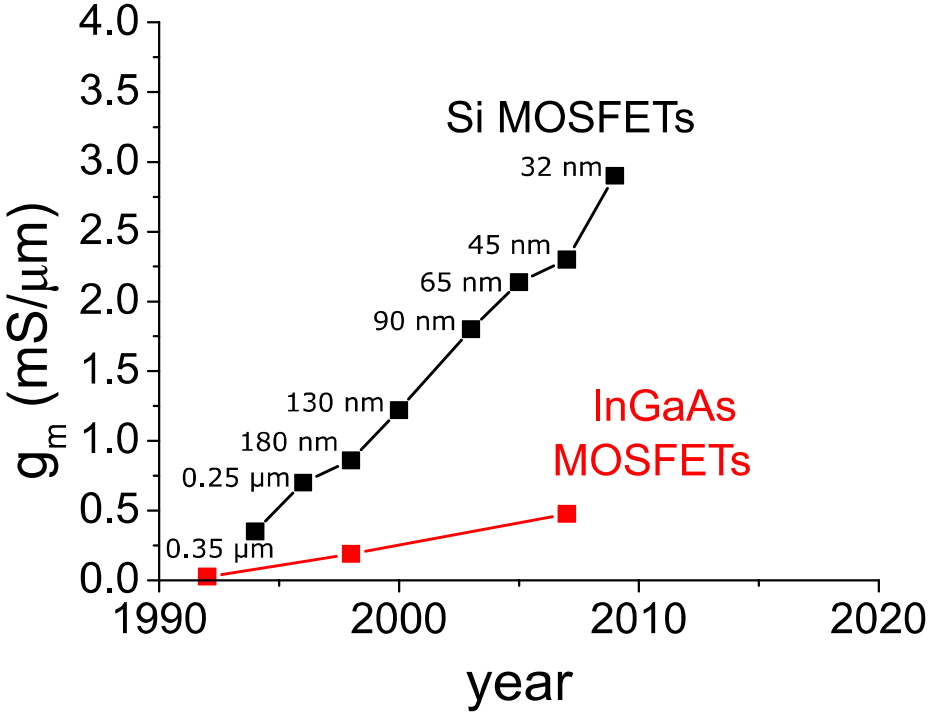
n-MOSFETs in Intel's nodes at nominal voltage



"Comparisons always fraught with danger…"

Transconductance of Planar Si vs. InGaAs MOSFETs

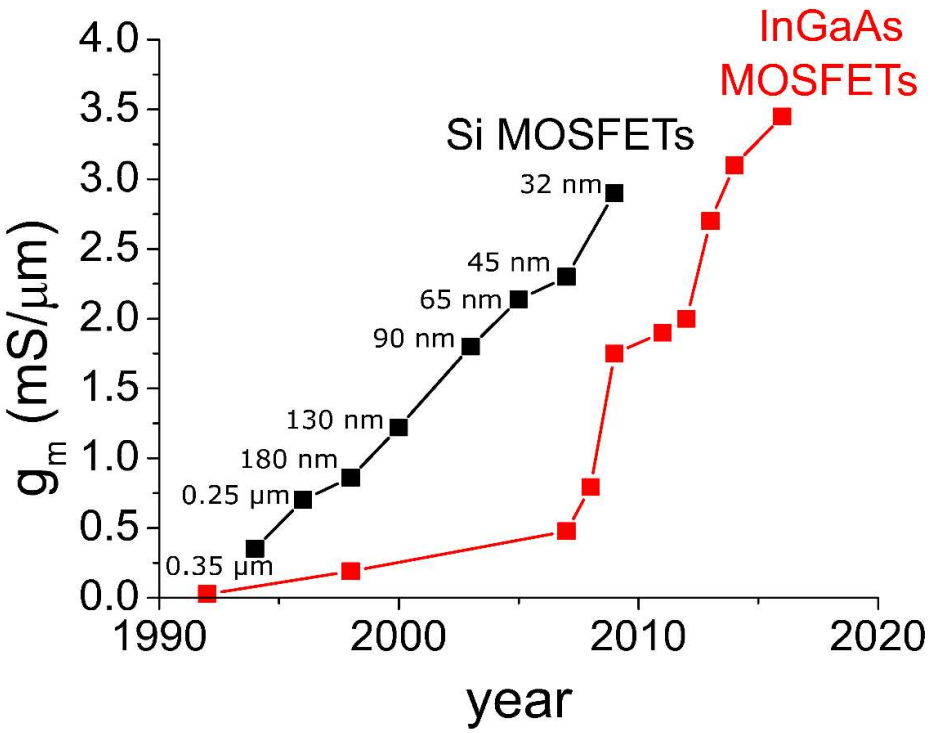
n-MOSFETs in Intel's nodes at nominal voltage



- InGaAs stagnant for a long time

Transconductance of Planar Si vs. InGaAs MOSFETs

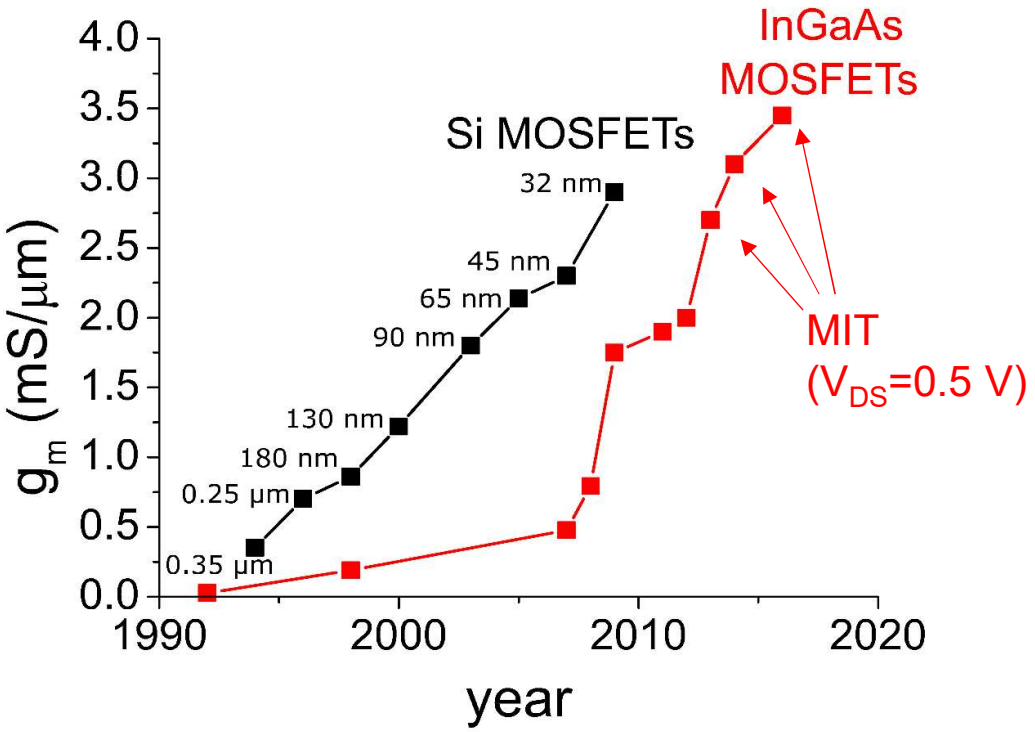
n-MOSFETs in Intel's nodes at nominal voltage

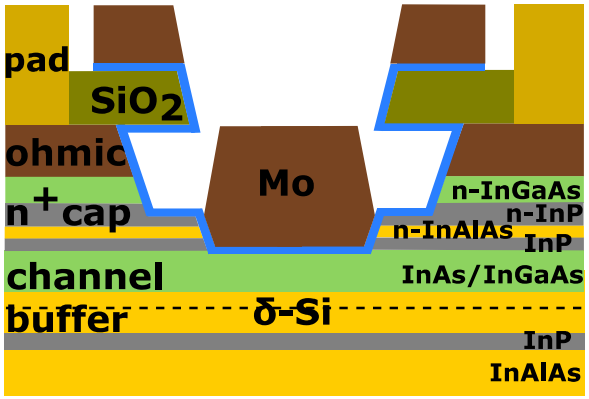


- Rapid recent progress → Atomic Layer Deposition
- InGaAs exceeds Si

Transconductance of Planar Si vs. InGaAs MOSFETs

n-MOSFETs in Intel's nodes at nominal voltage





Lin, IEDM 2014, EDL 2016

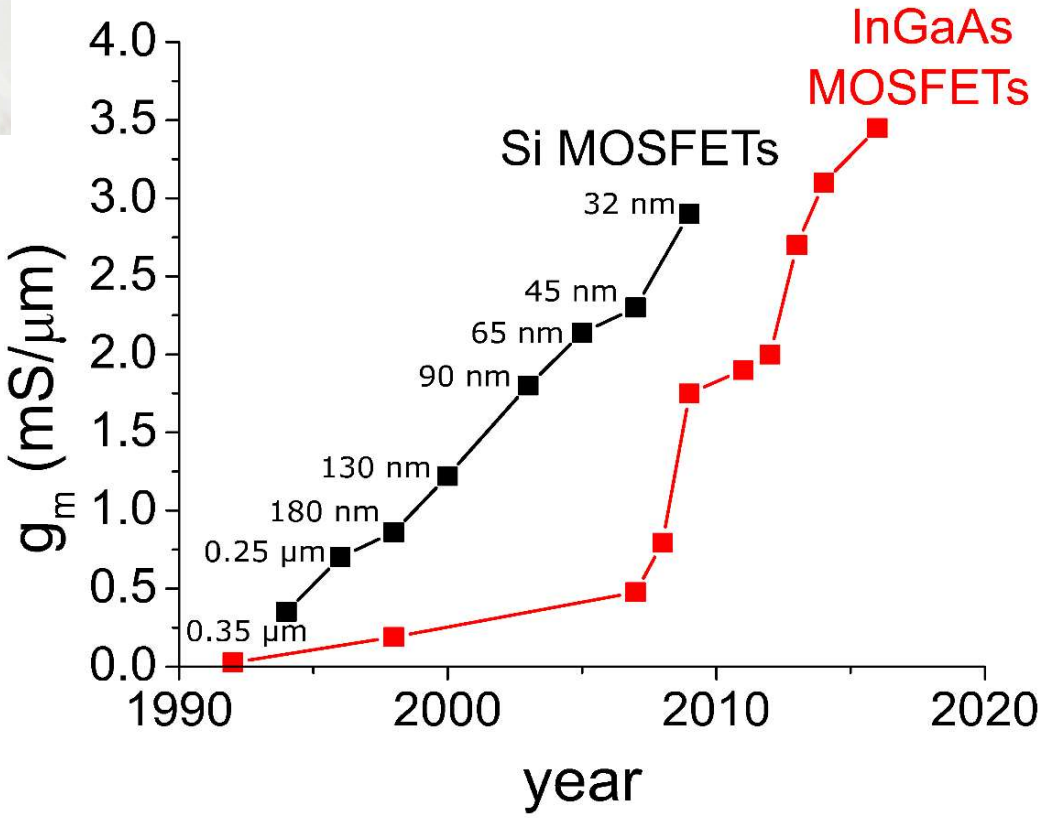
- Rapid recent progress → Atomic Layer Deposition
- InGaAs exceeds Si

Evolution of transistor structure for improved scalability

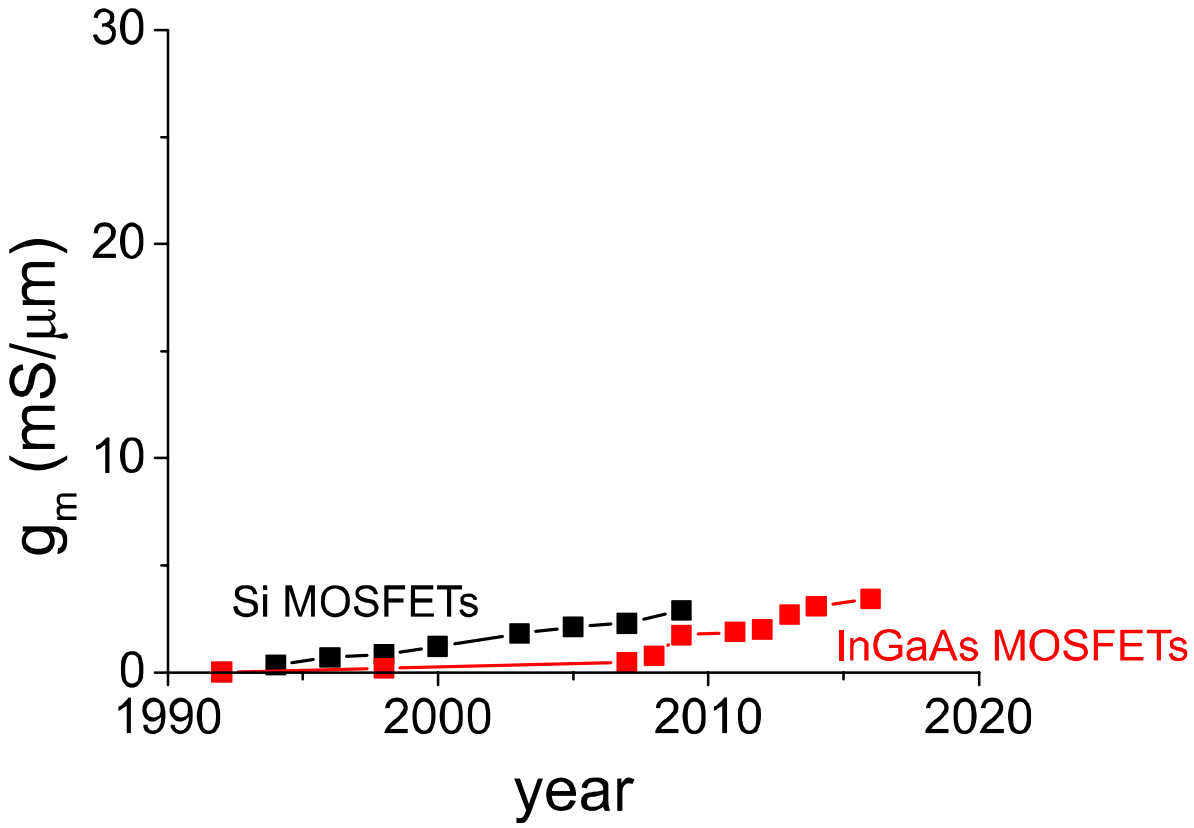
FinFET

Enhanced gate control → improved scalability

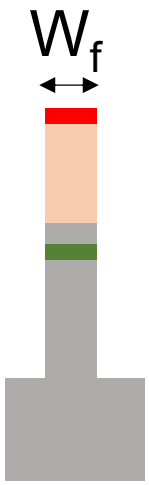
Transconductance of planar Si vs. InGaAs MOSFETs



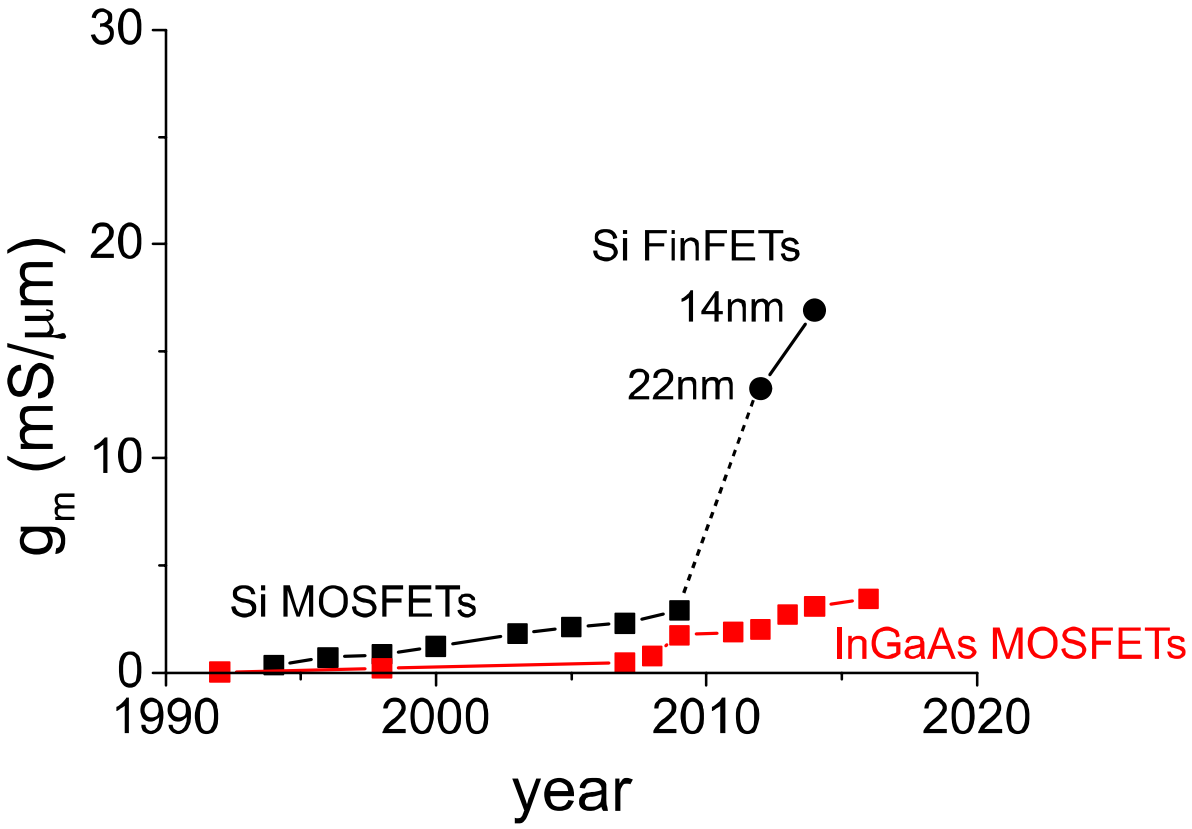
Transconductance of Si vs. InGaAs FinFETs



Transconductance of Si vs. InGaAs FinFETs

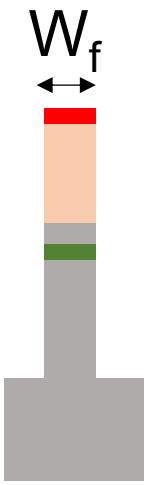


g_m normalized by fin width

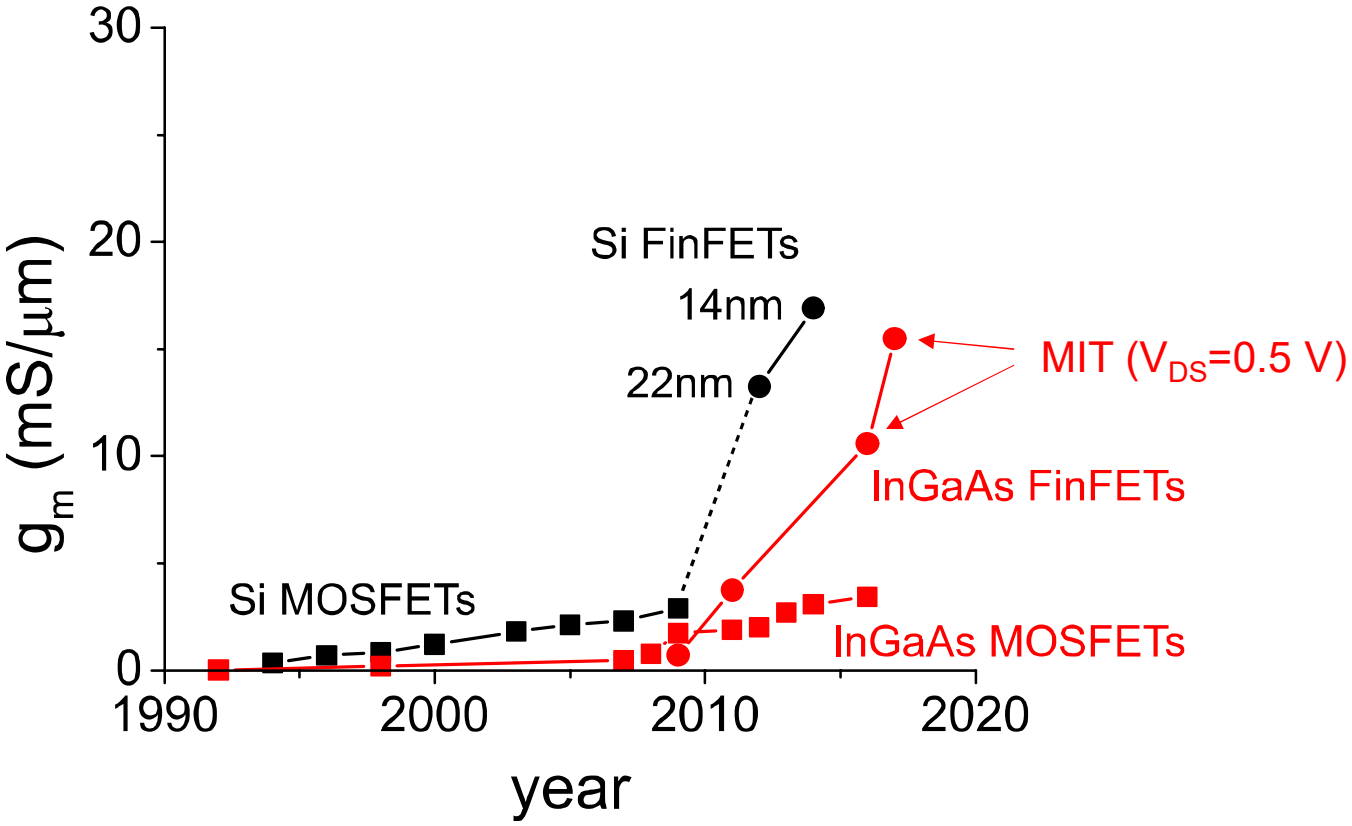


FinFET: large increase in current density per unit footprint over planar MOSFET

Transconductance of Si vs. InGaAs FinFETs

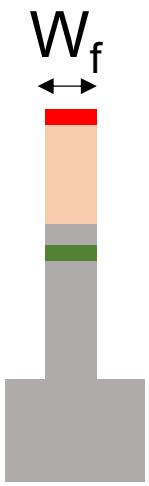


g_m normalized by fin width

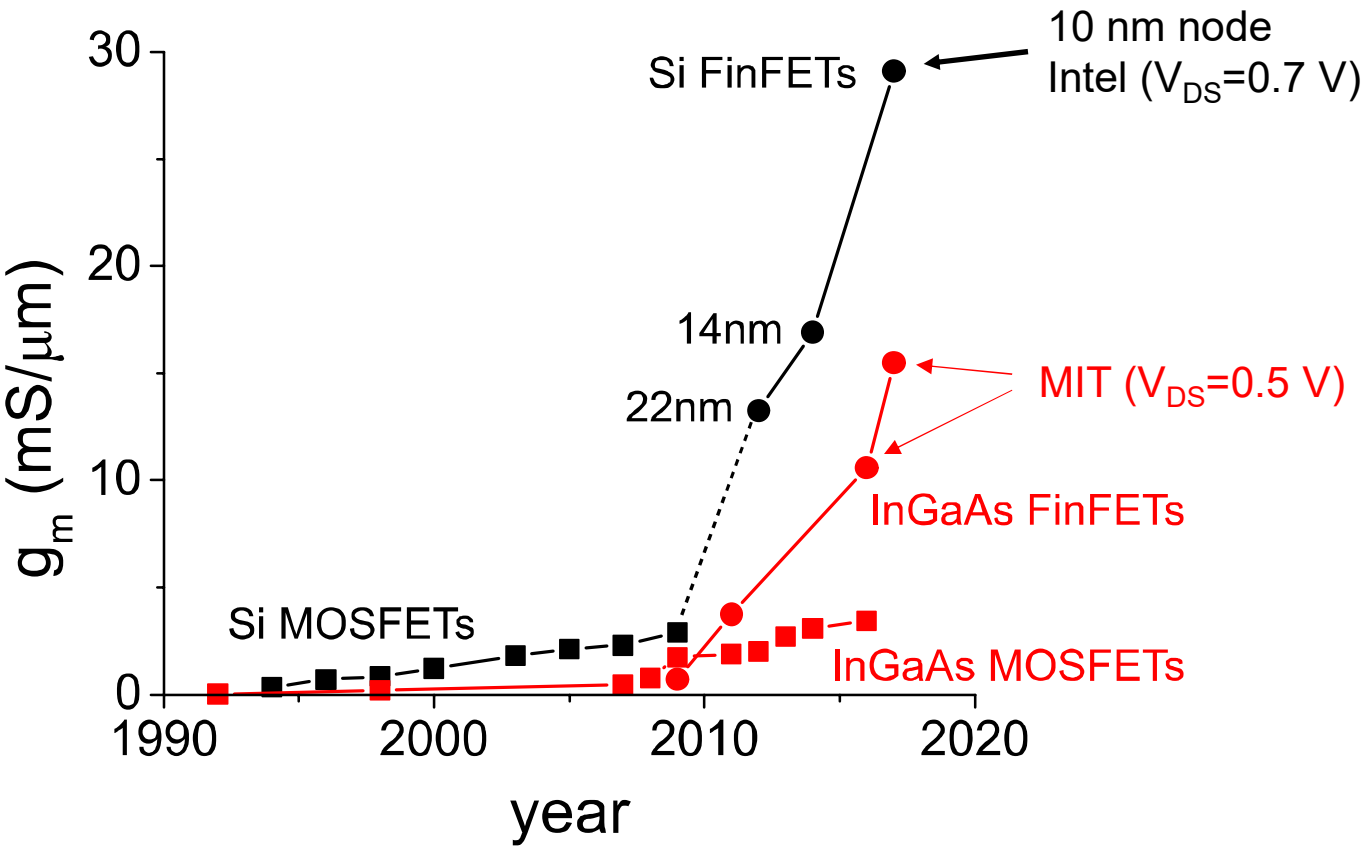


Best InGaAs FinFETs nearly match 14 nm Si MOSFETs

Transconductance of Si vs. InGaAs FinFETs



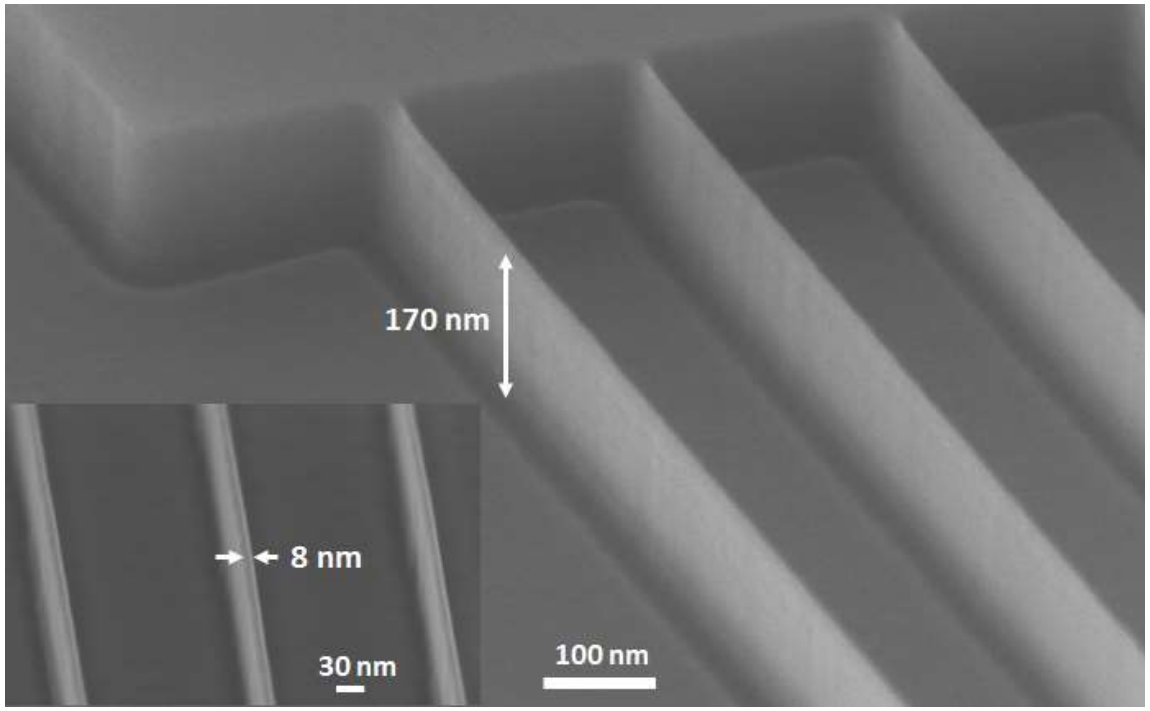
g_m normalized by fin width



10 nm node Si MOSFETs: a great new challenge!

InGaAs FinFETs @ MIT

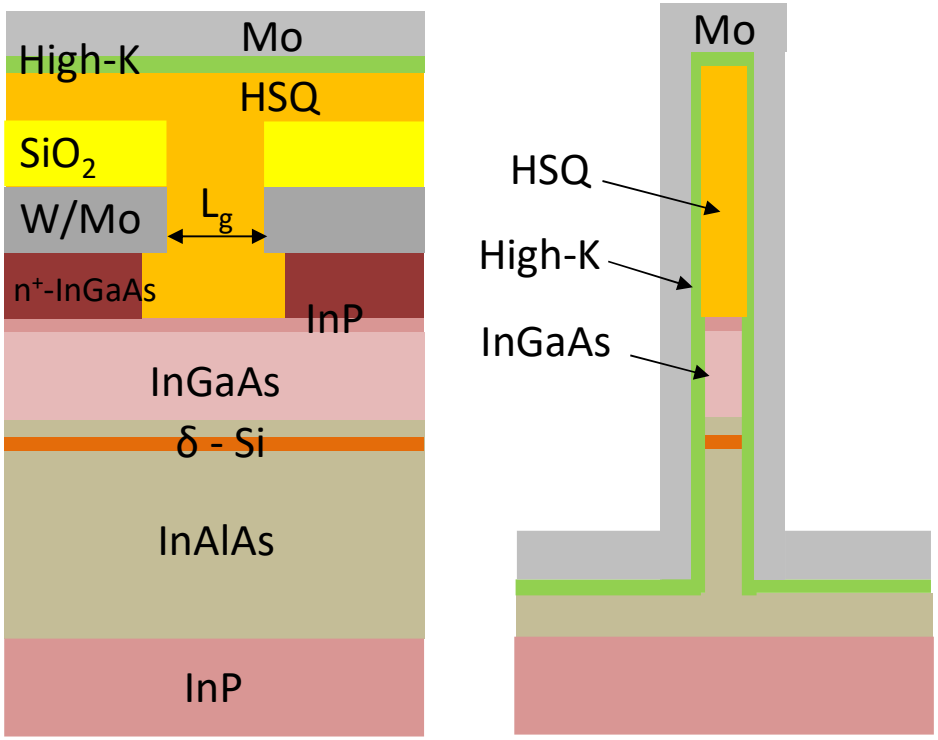
Key enabling technologies: $BCl_3/SiCl_4/Ar$ RIE + digital etch

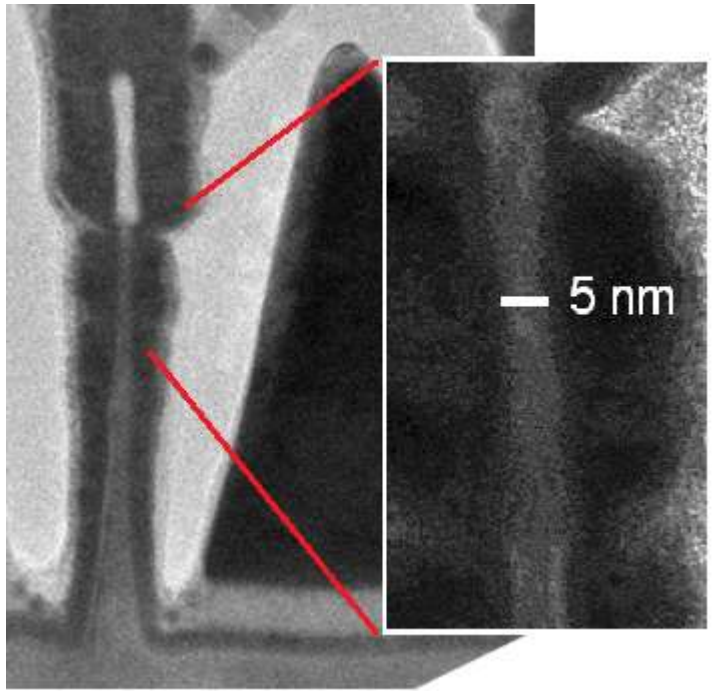


- Sub-10 nm fin width
- Aspect ratio > 20
- Vertical sidewalls

Vardi,
DRC 2014,
EDL 2015,
IEDM 2015

InGaAs FinFETs @ MIT



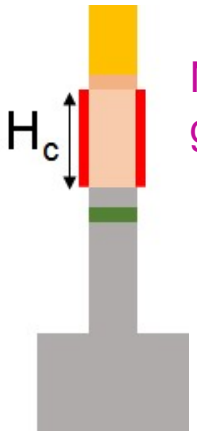


Vardi, IEDM 2017

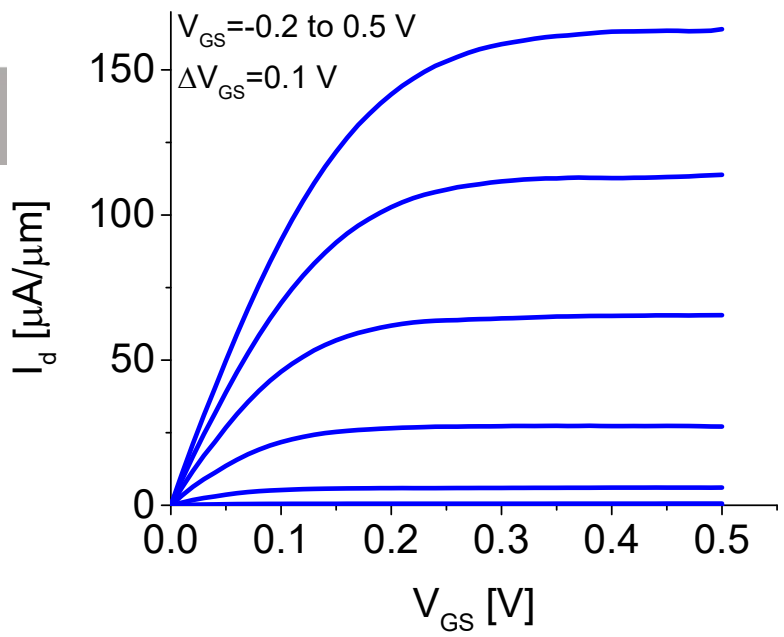
- Si-compatible process
- Contact-first, gate-last process
- Fin etch mask left in place → double-gate MOSFET

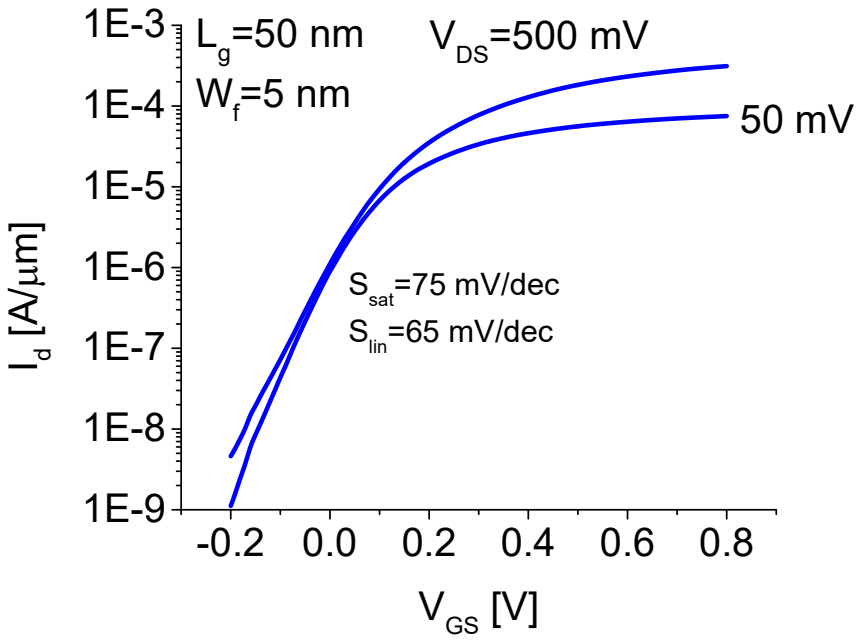
Most aggressively scaled FinFET

W_f=5 nm, L_g=50 nm, H_c=50 nm (AR=10), EOT=0.8 nm:



Normalized by conducting gate periphery = $2H_c$

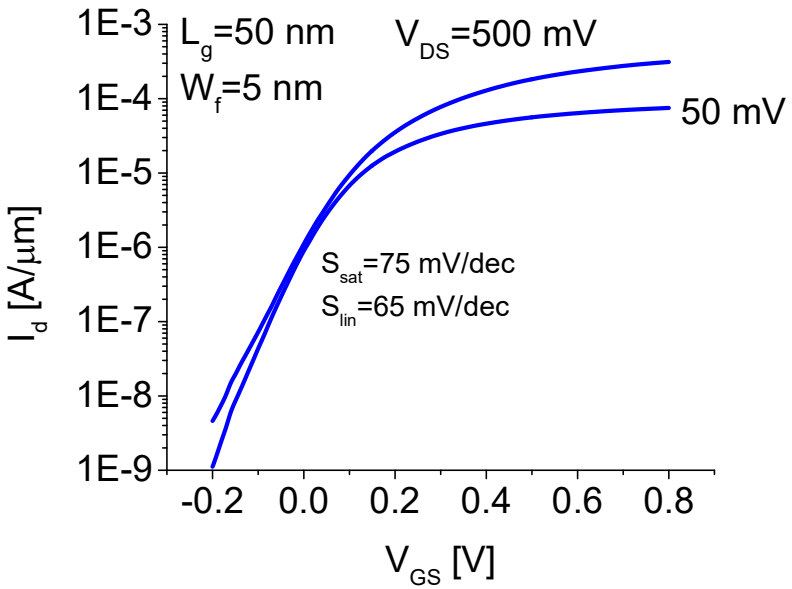


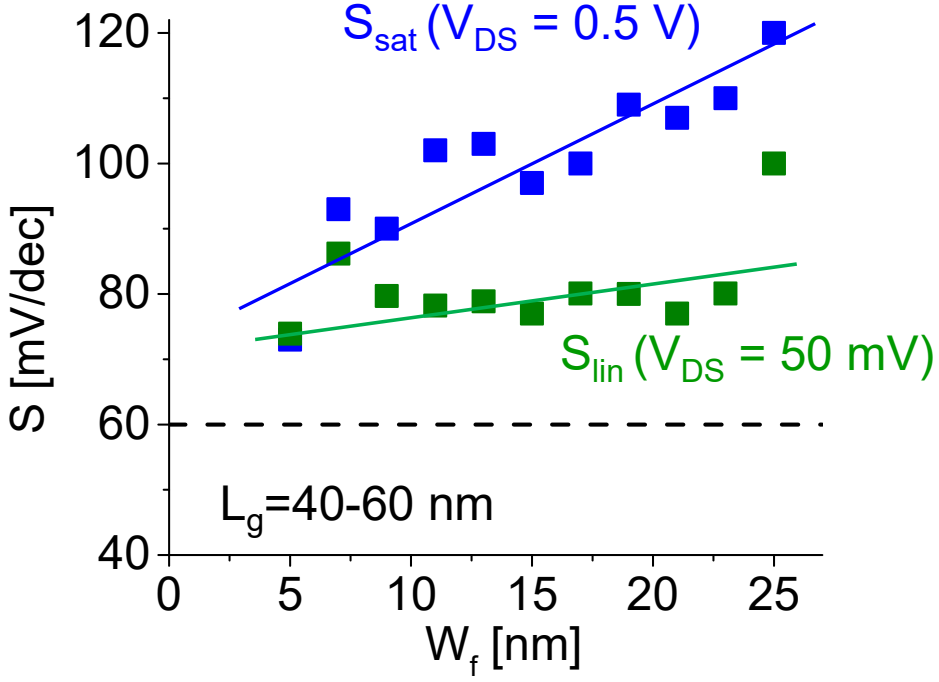


Vardi, IEDM 2017

$g_{m,max}$=565 μS/μm (V_{DS}=0.5 V)

W_f scaling of OFF-state characteristics

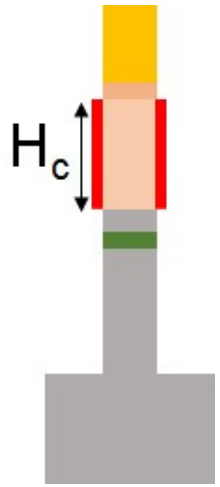




- Excellent subthreshold swing scaling behavior
- From long L_g devices: D_{it} ~ $8x10^{11}$ $cm^{-2}.eV^{-1}$

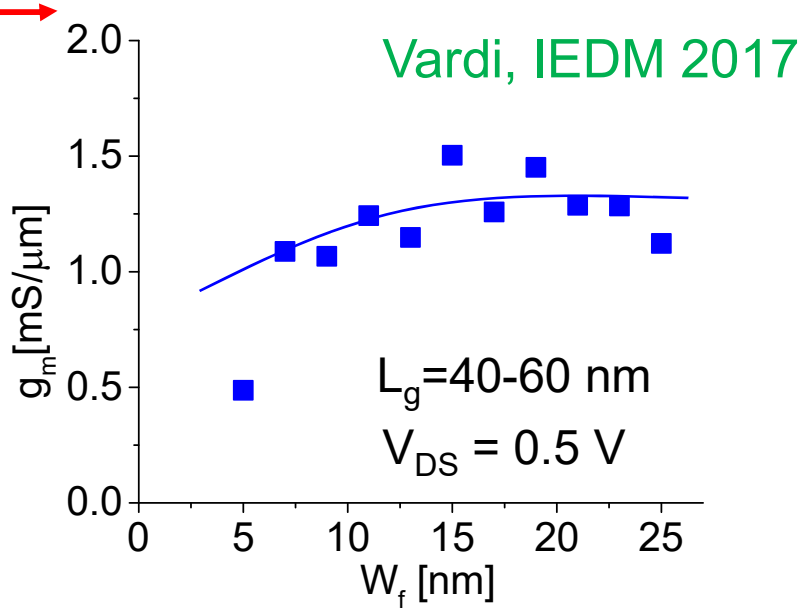
Vardi, IEDM 2017

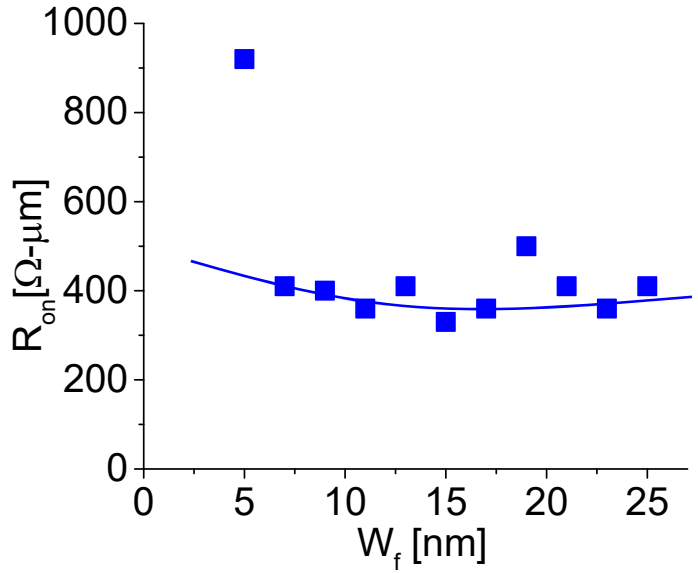
W_f scaling of ON-state characteristics



Normalized by conducting gate periphery = $2H_c$

in planar MOSFETs expect 2.2 mS/μm

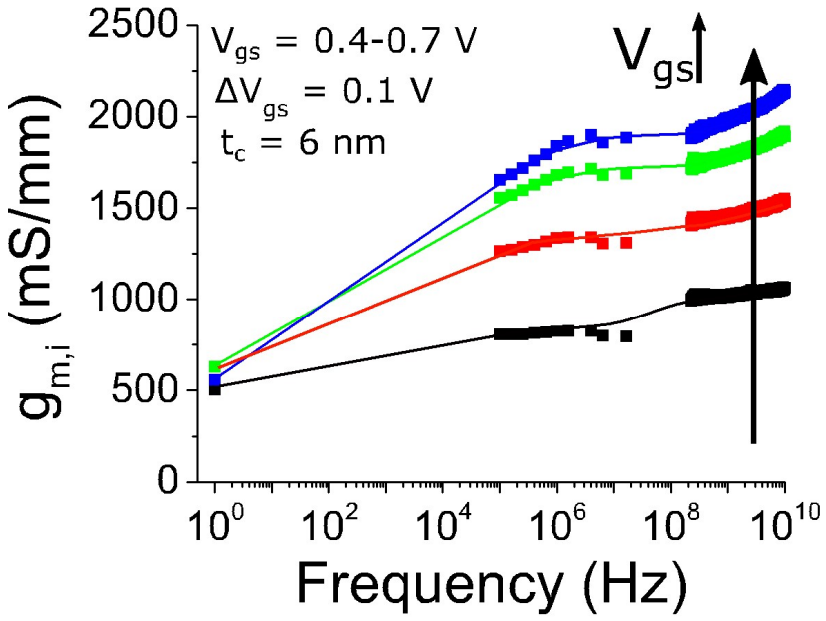




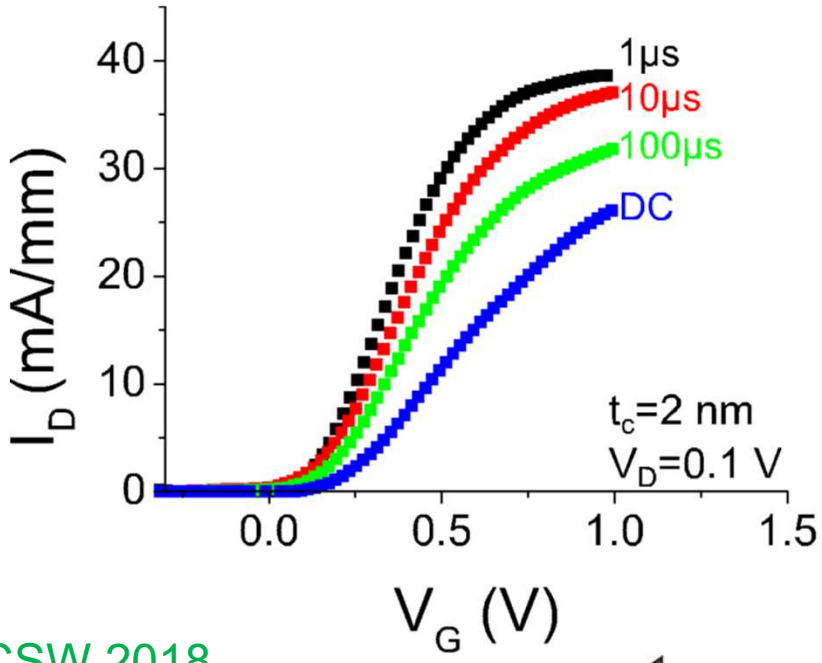
- g_m independent of W_f down to W_f=7 nm
- In planar MOSFET (x=0.53) expect g_m~ 2.2 mS/μm
- Missing performance hints at sidewall damage

DC underestimates transistor potential!

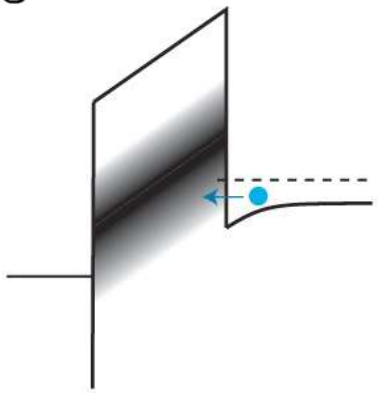
g_m frequency dispersion



Pulsed vs. DC

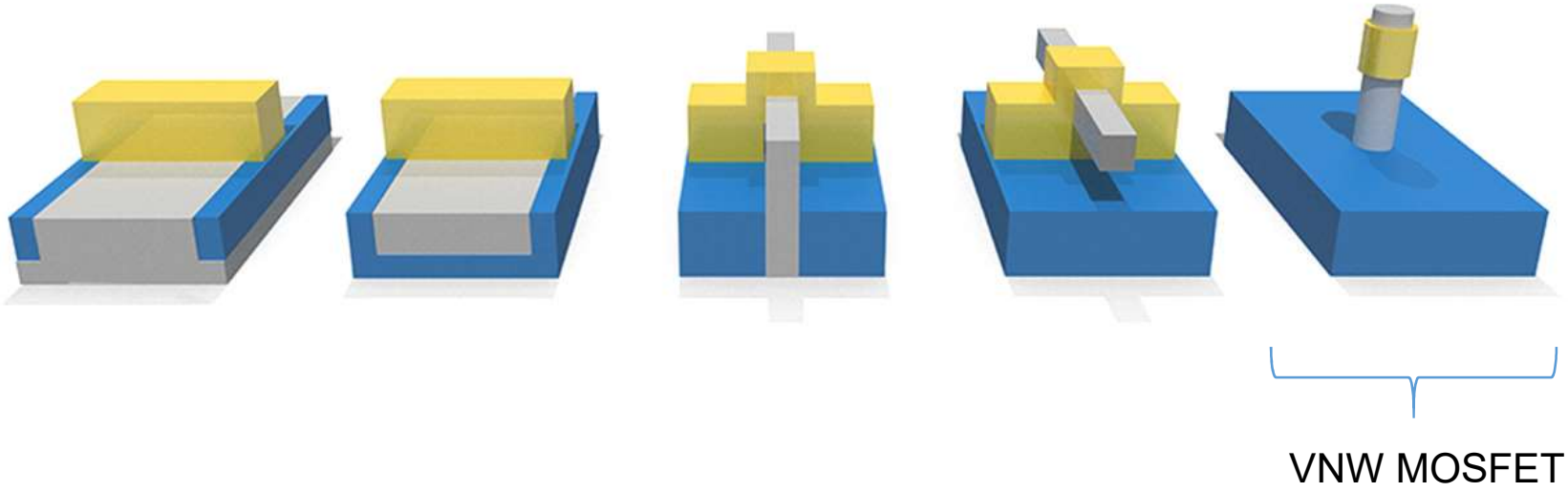


Cai, CSW 2018



- Severe frequency dispersion in g_m
- Pulsed I-V ≠ DC I-V
- Due to gate oxide trapping

InGaAs Vertical Nanowire MOSFETs

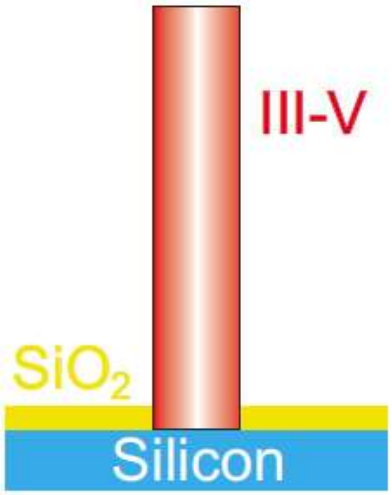


Vertical NW MOSFET:

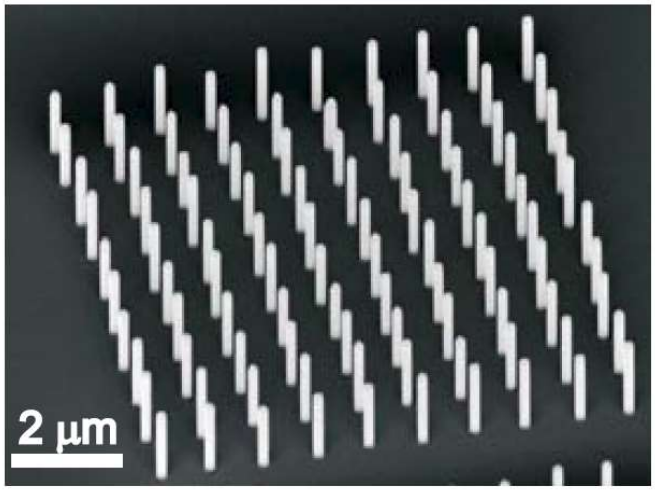
→ ultimate scalable transistor

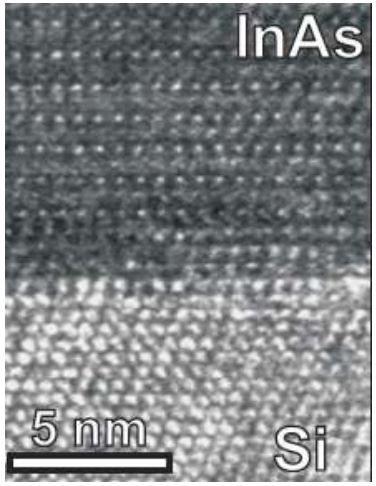
→ uncouples footprint scaling from L_g, L_{spacer}, and L_c scaling

InGaAs Vertical Nanowires on Si by direct growth



Selective-Area Epitaxy (SAE)

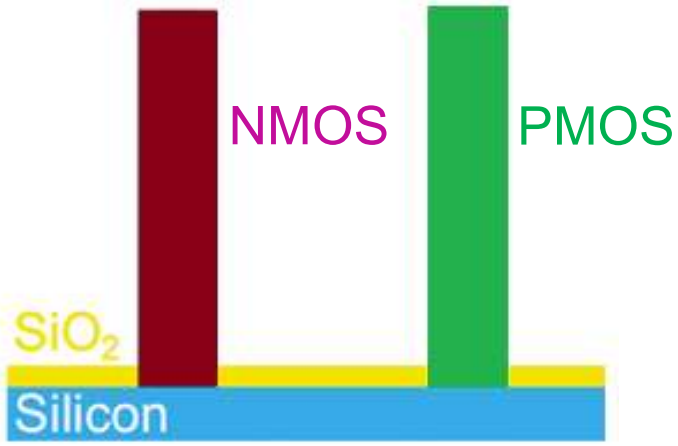




InAs NWs on Si by SAE

Riel, MRS Bull 2014, IEDM 2012

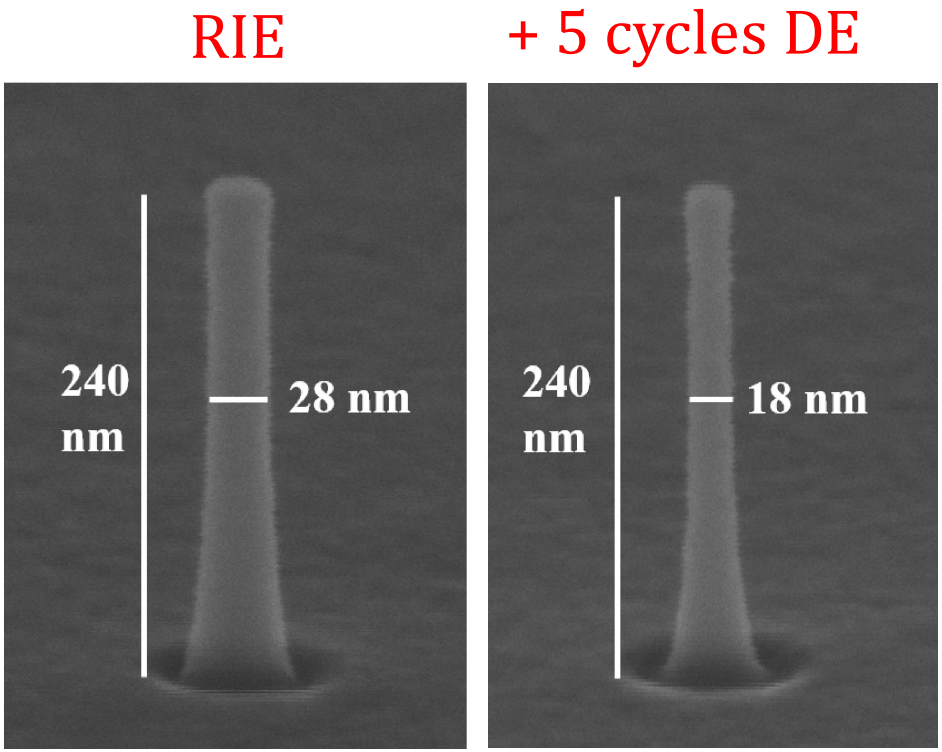
VNW MOSFETs: path for III-V integration on Si for future CMOS



InGaAs VNWs by top-down approach

Key enabling technologies: $BCl_3/SiCl_4/Ar$ RIE + digital etch

DE = O_2 plasma oxidation + acid-based oxide removal



Zhao, EDL 2014

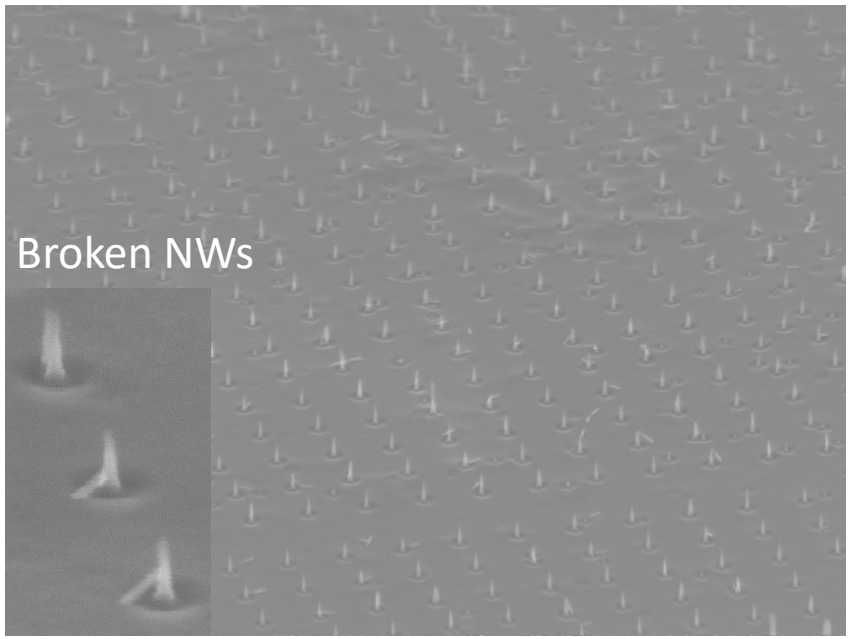
Radial etch rate = 1 nm/cycle

Towards D<10 nm InGaAs VNWs

RIE down to D~20 nm + multiple cycles of DE

8 nm InGaAs VNWs after 7 DE cycles:

Lu, EDL 2017



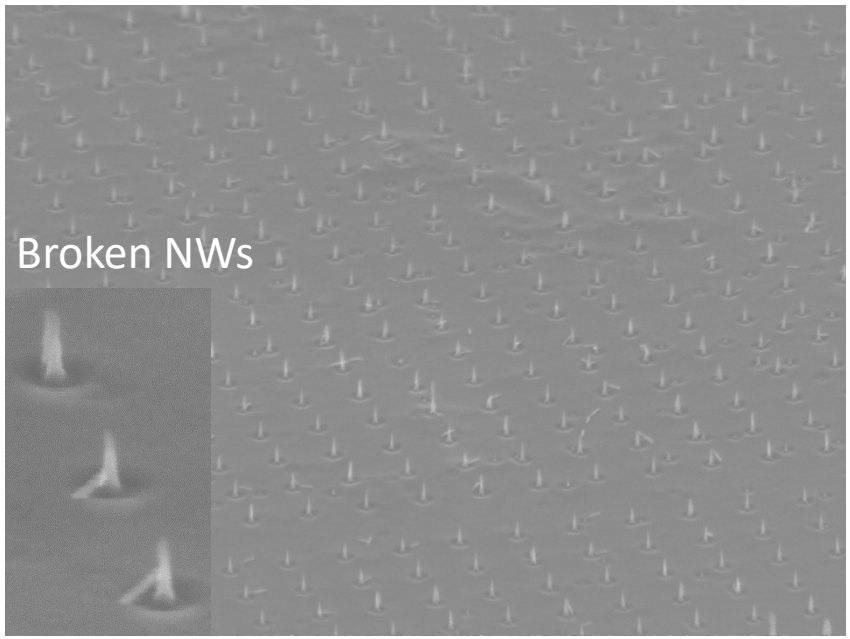
10% HCl in DI water, Yield = 0%

Towards D<10 nm InGaAs VNWs

RIE down to D~20 nm + multiple cycles of DE

8 nm InGaAs VNWs after 7 DE cycles:

Lu, EDL 2017



10% HCl in DI water, Yield = 0%

Water-based acid is problem:

Surface tension (mN/m):

- Water: 72
- Methanol: 22
- IPA: 23

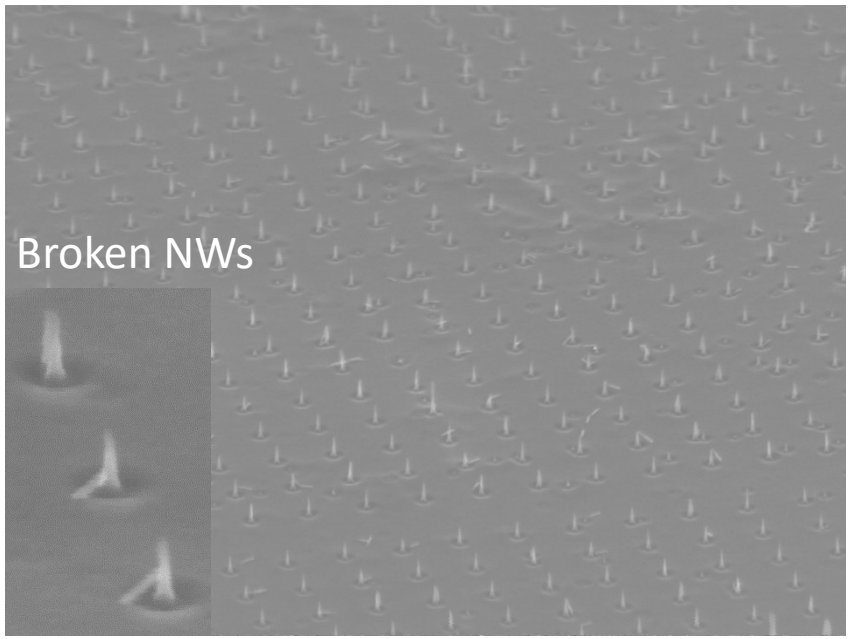
Solution: *alcohol-based digital etch*

Towards D<10 nm InGaAs VNWs

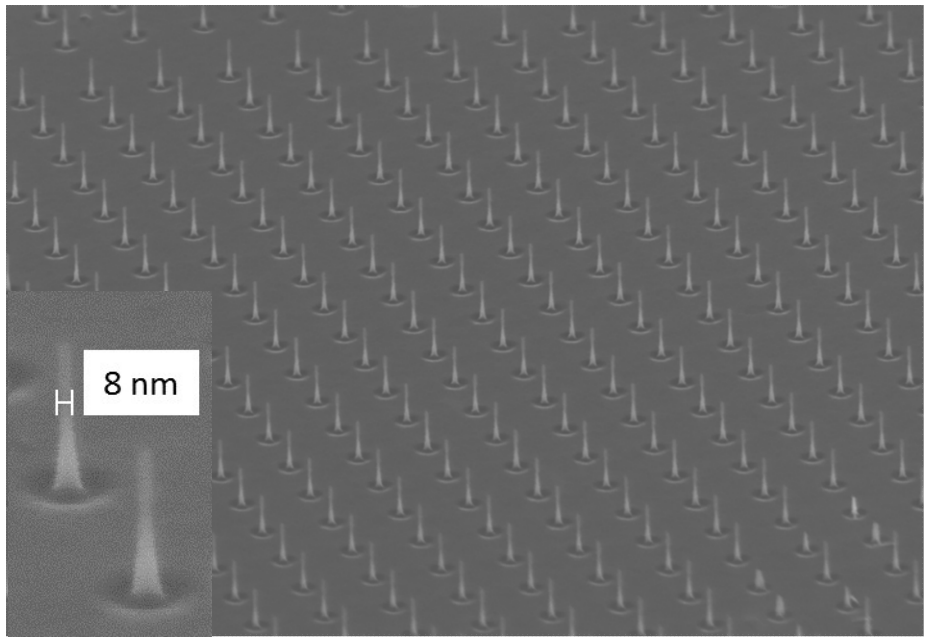
RIE down to D~20 nm + multiple cycles of DE

8 nm InGaAs VNWs after 7 DE cycles:

Lu, EDL 2017



10% HCl in DI water, Yield = 0%

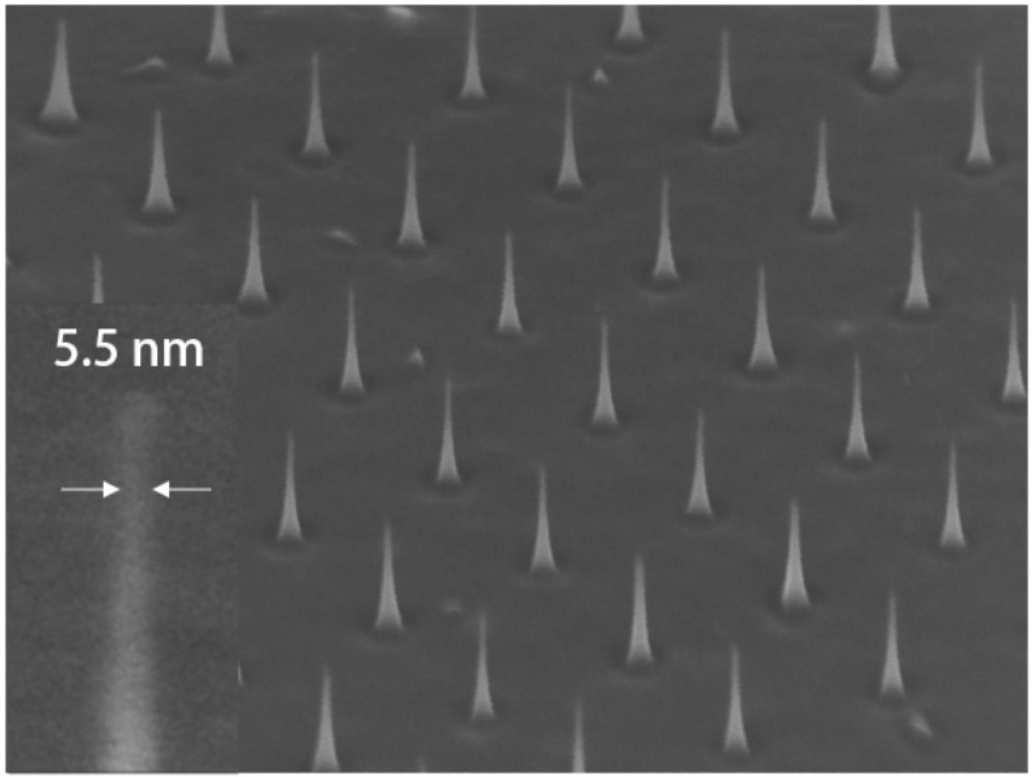


10% HCl in IPA, Yield = 97%

Alcohol-based DE key for D < 10 nm

D=5.5 nm InGaAs VNW arrays

10% H_2SO_4 in methanol

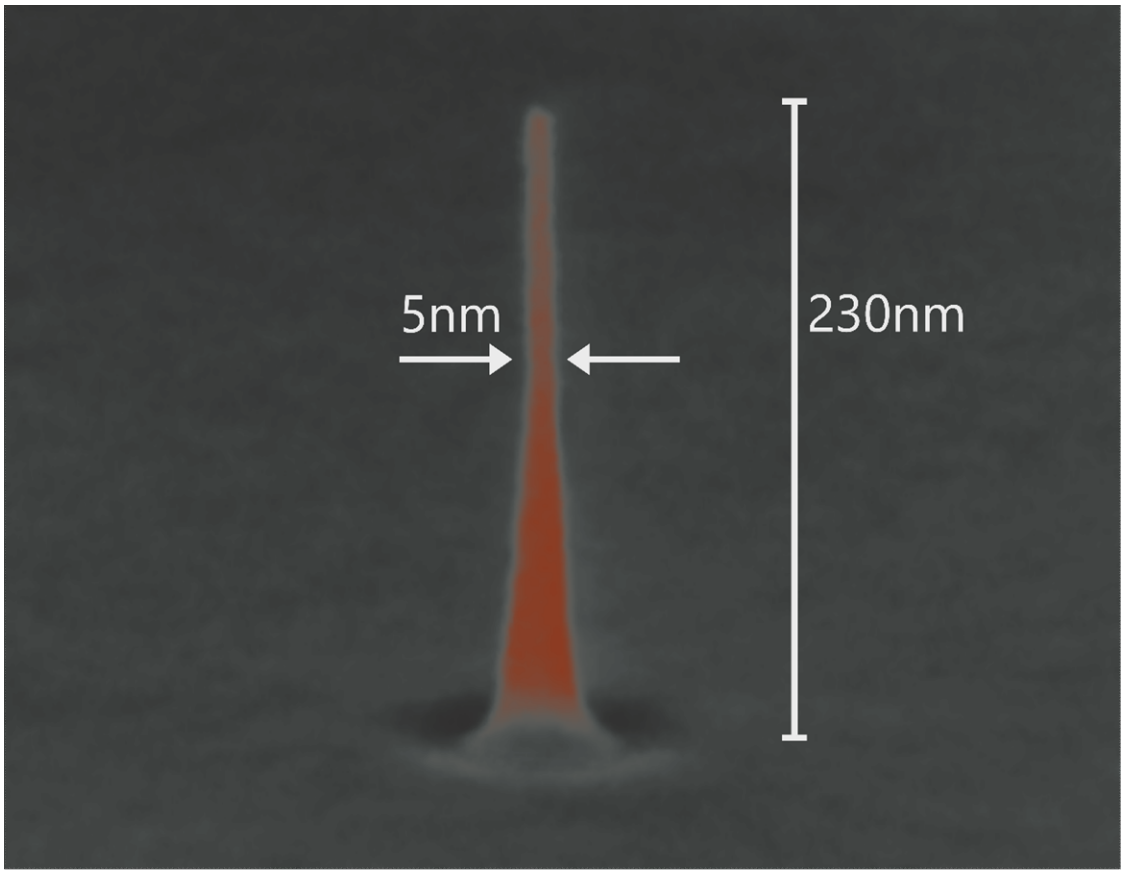


90% yield

Lu, EDL 2017

- H_2SO_4:methanol yields 90% at D=5.5 nm!
- Viscosity matters: methanol (0.54 cP) vs. IPA (2.0 cP)

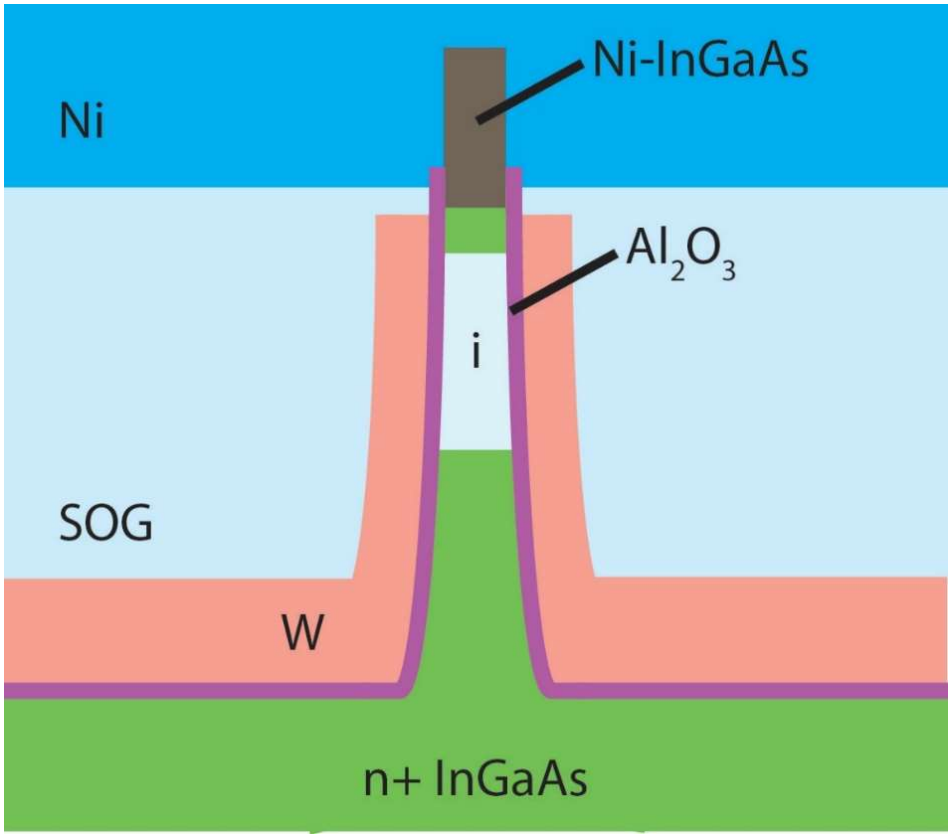
D=5 nm InGaAs VNW



Aspect Ratio > 40

Lu, EDL 2017

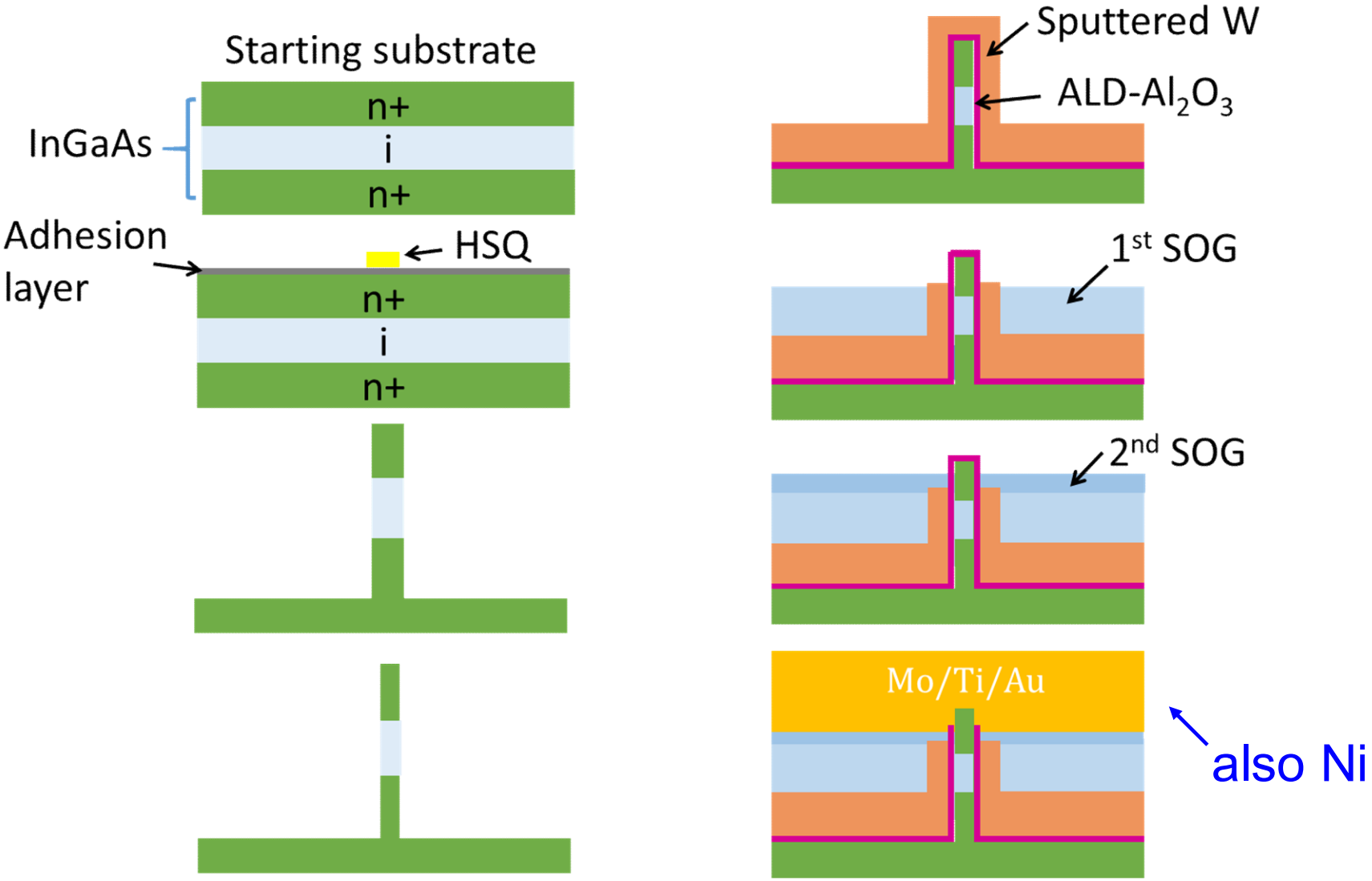
InGaAs VNW-MOSFETs by top-down approach @ MIT



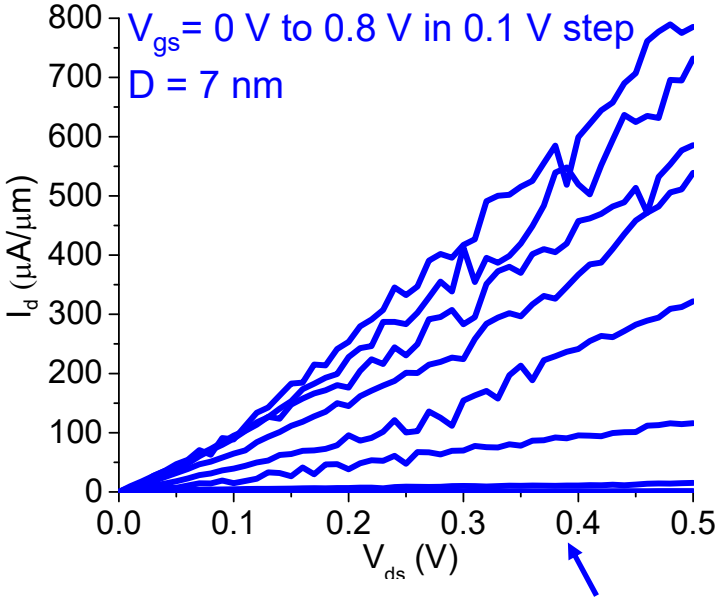
Zhao, IEDM 2017

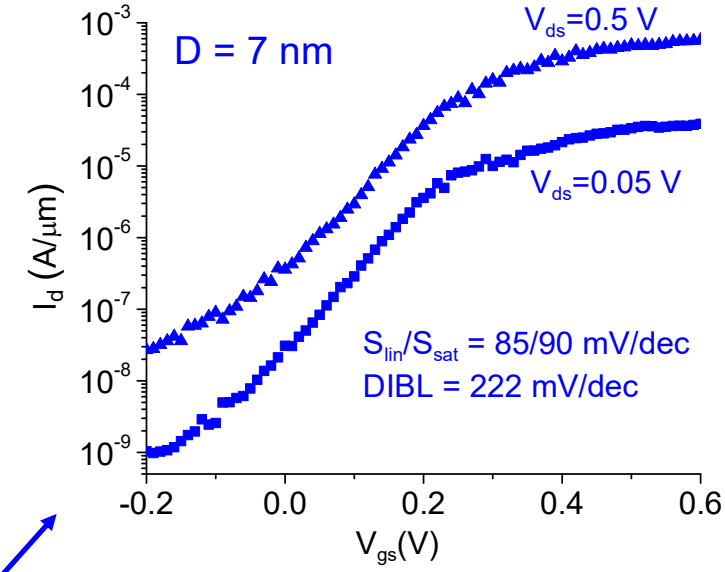
Top-down approach: flexible and manufacturable

III-V VNW MOSFET process flow



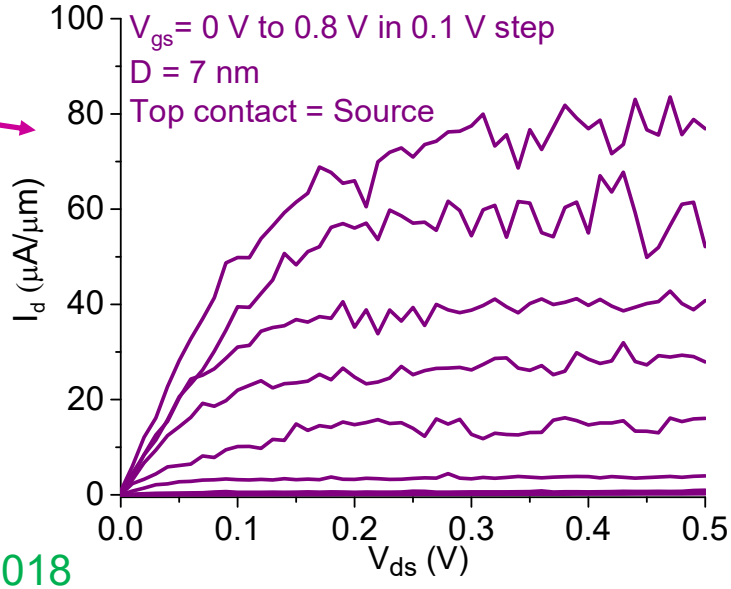
D=7 nm InGaAs VNW MOSFET (Ni contact)





Source down

Source up



- *Single* nanowire MOSFET (L_{ch}= 80 nm)
- First sub-10 nm diameter VNW FET of any kind on any material system

Zhao, IEDM 2017, TED 2018

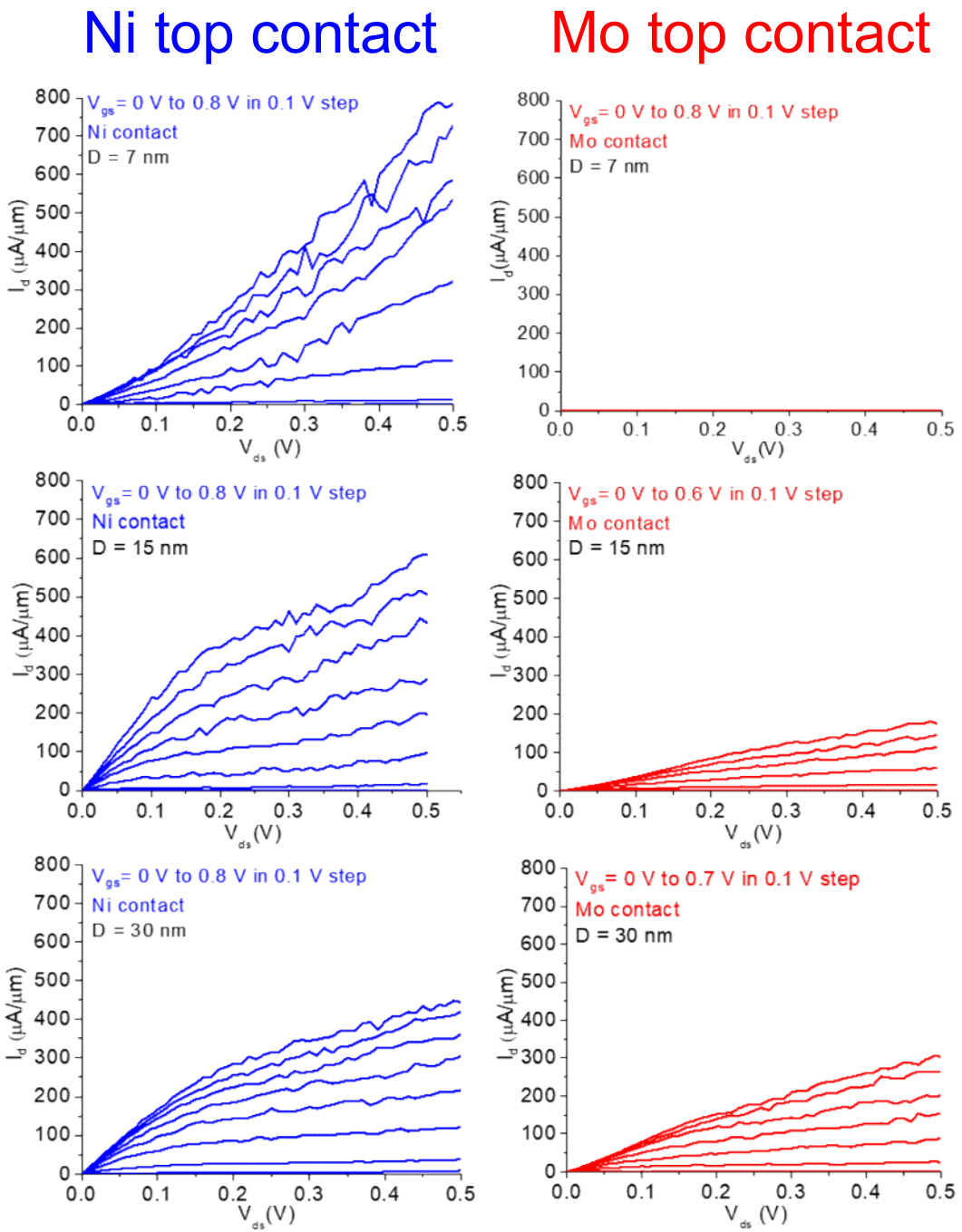
Output characteristics vs. D (source up)

Source up:

As D↓:

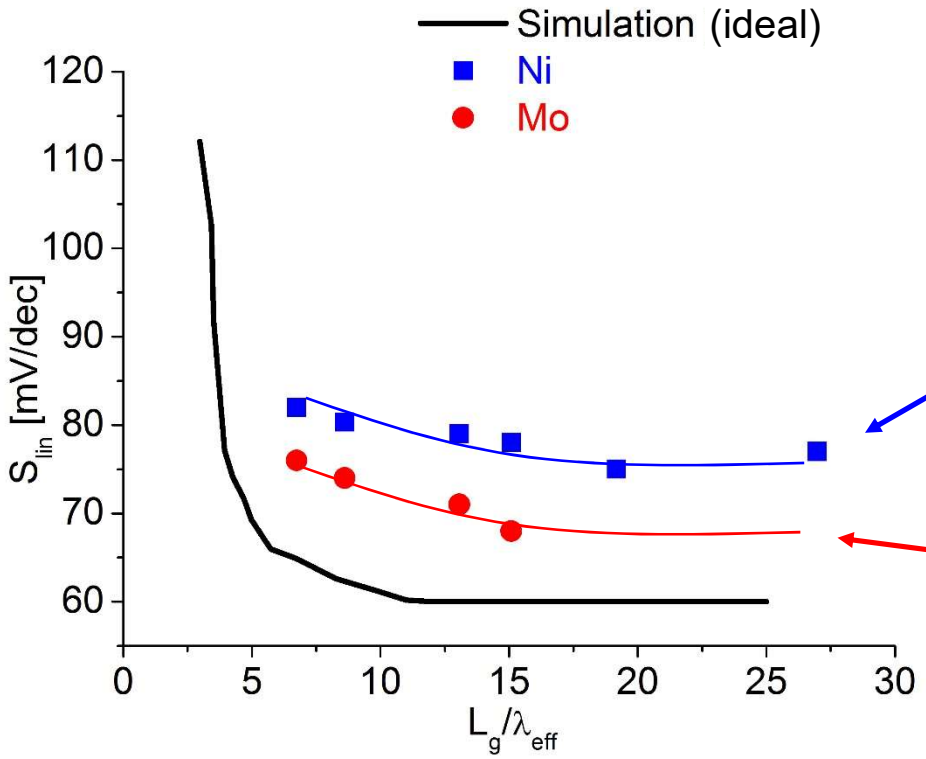
- Ni contact becomes Schottky
- Mo contact opens up

Zhao, TED 2018



Sidewall MOS interface quality

Subthreshold swing vs. electrostatic aspect ratio of channel:



Zhao, TED 2018

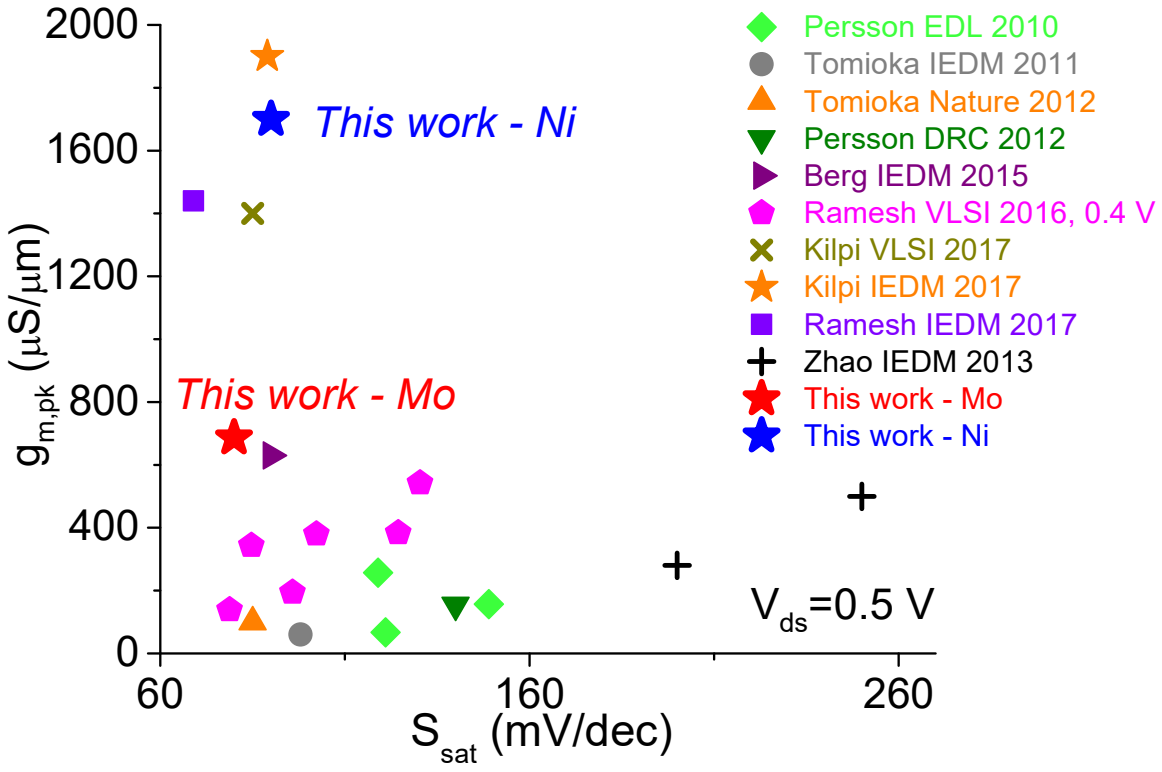
$D_{it} \sim 6x10^{12}$ cm^{-2}.eV^{-1}
(200^{o}C RTA)

$D_{it} \sim 4x10^{12}$ cm^{-2}.eV^{-1}
(300^{o}C RTA)

Poor MOS interface at sidewall

Benchmark with Si/Ge VNW MOSFETs

Peak g_m (V_{DS}=0.5 V) vs. S_{sat} of InGaAs VNW MOSFETs

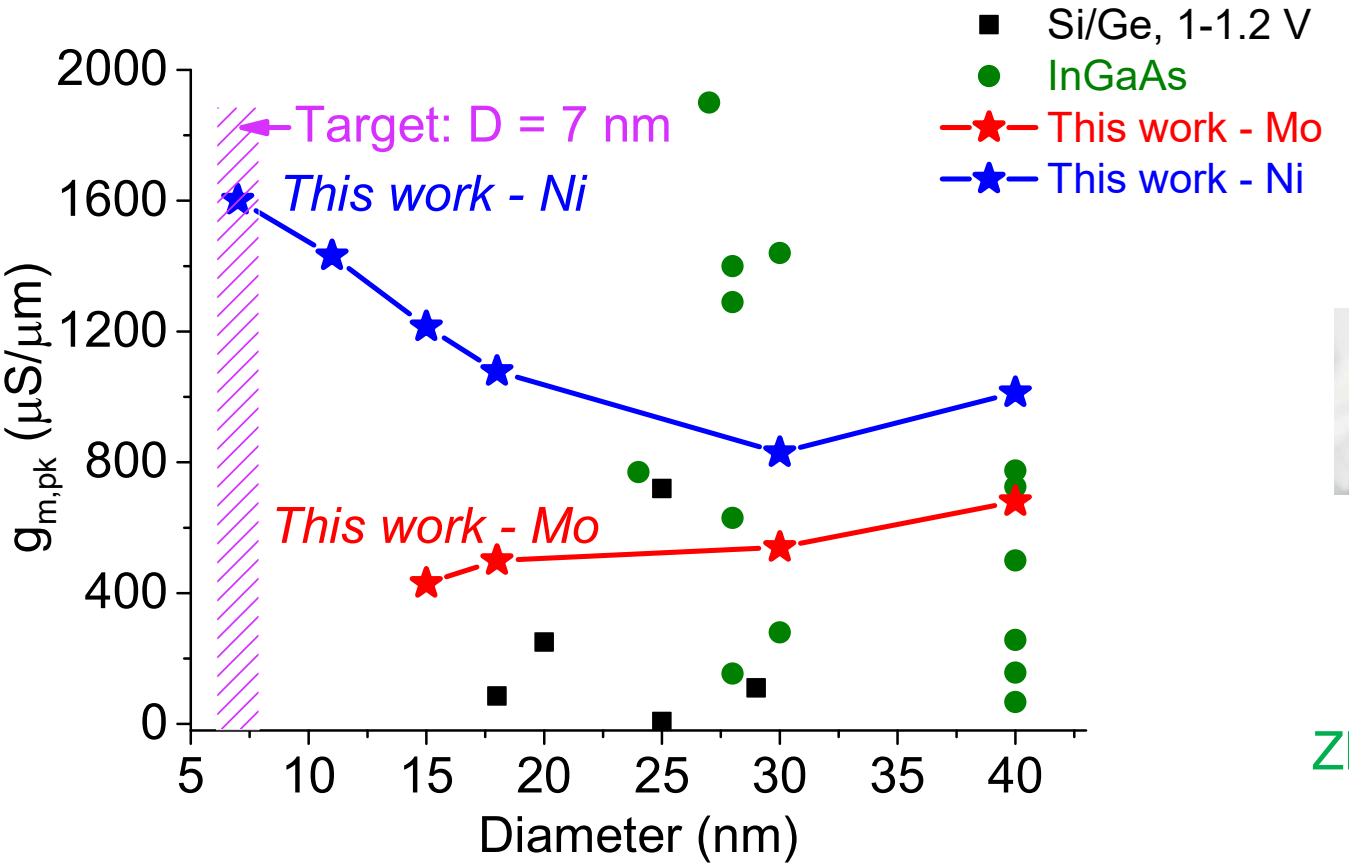


Zhao, IEDM 2017

Excellent combination of on-and off-state characteristics

Benchmark with Si/Ge VNW MOSFETs

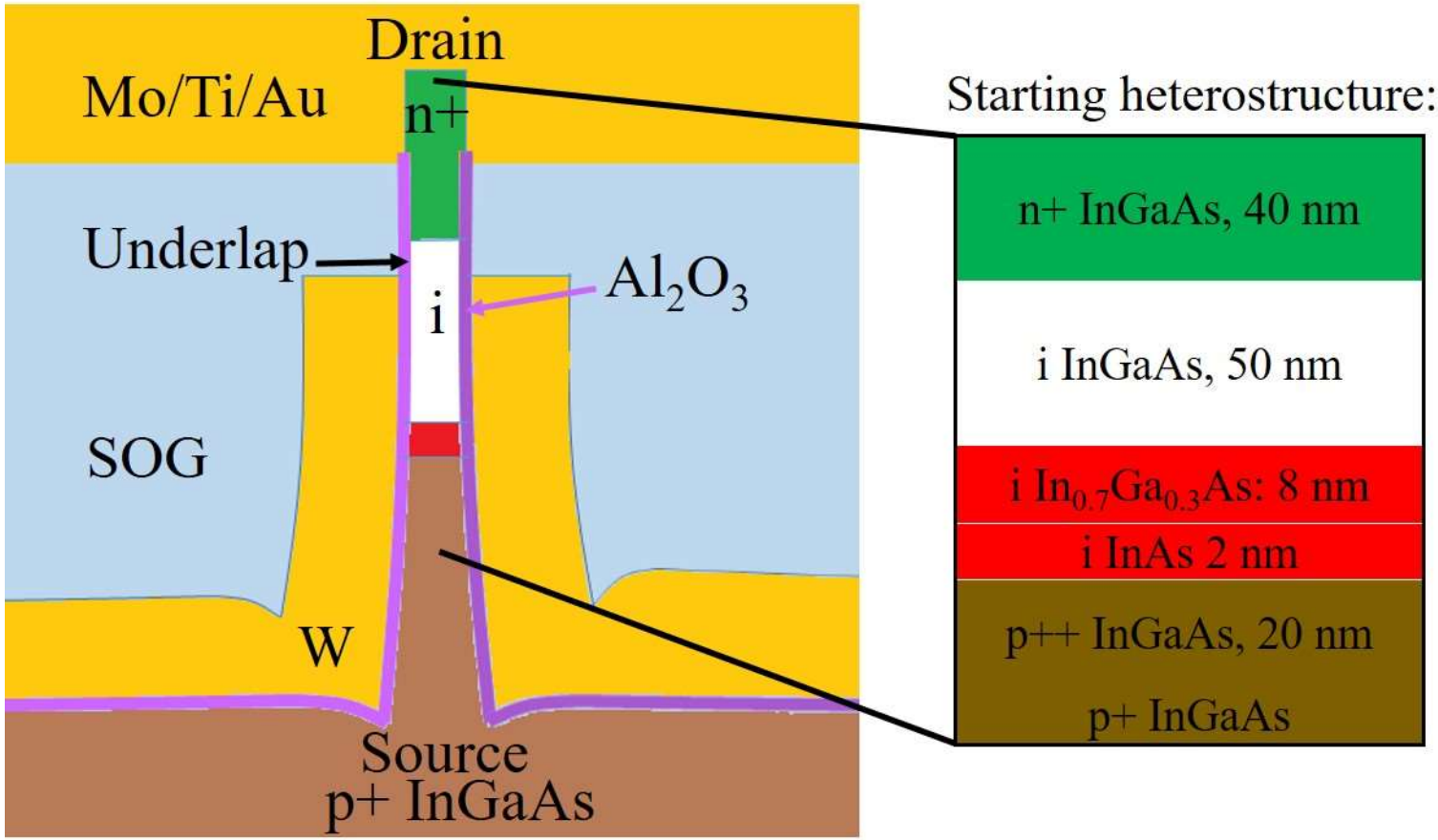
Peak g_m of InGaAs (V_{DS}=0.5 V), Si and Ge VNW MOSFETs



Zhao, IEDM 2017

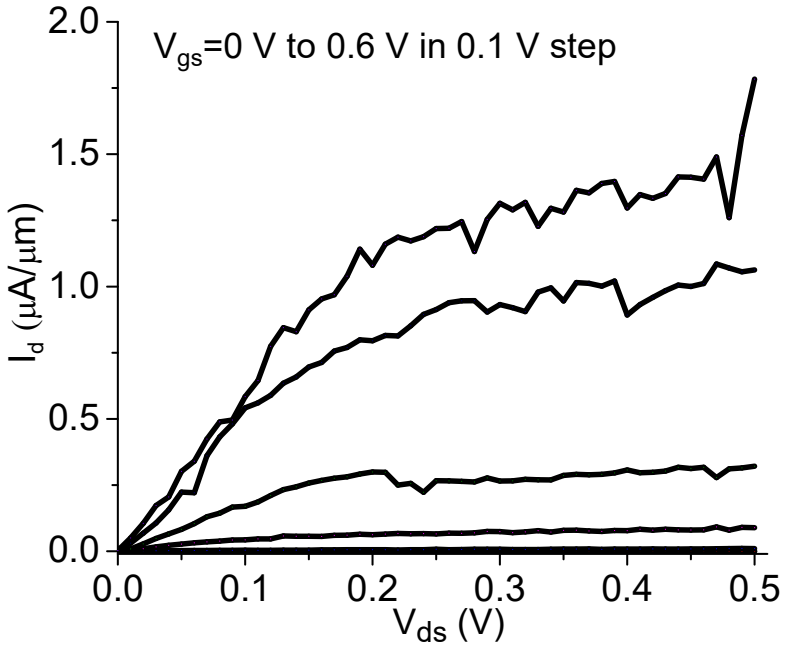
InGaAs competitive with Si [hard to add strain]

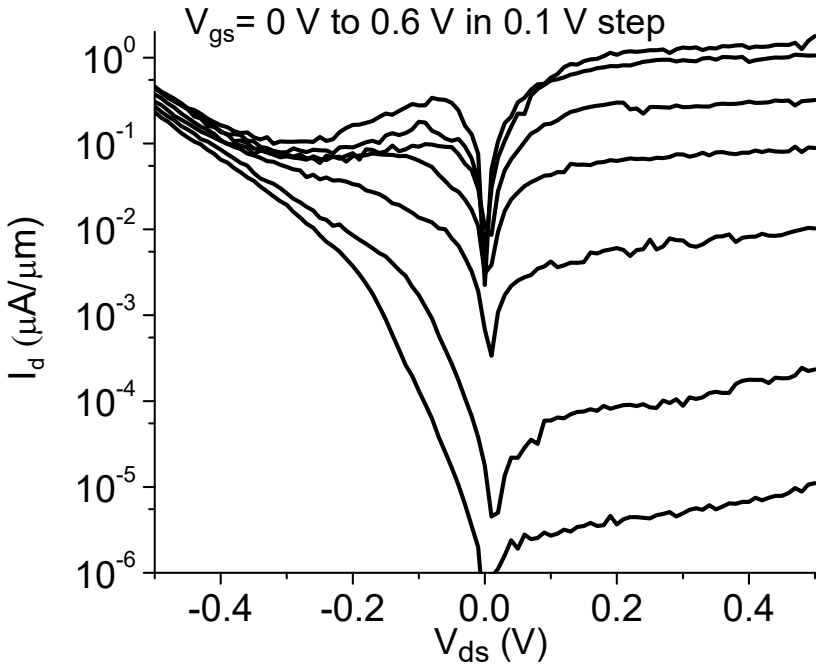
InGaAs/InAs VNW Tunnel FETs @ MIT



InGaAs VNW-TFET

Single NW: D= 40 nm, L_{ch}= 60 nm, 3 nm Al_2O_3 (EOT = 1.5 nm)

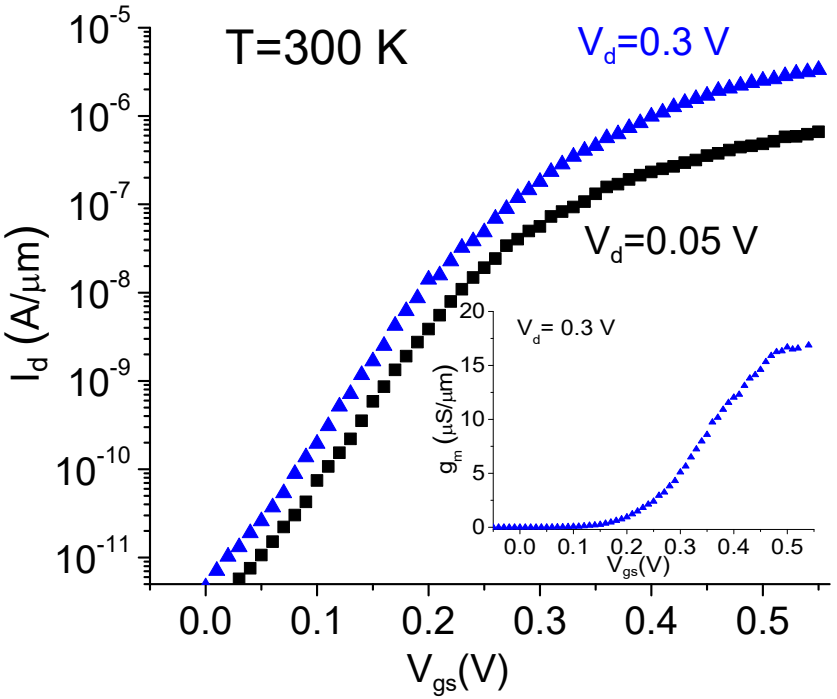


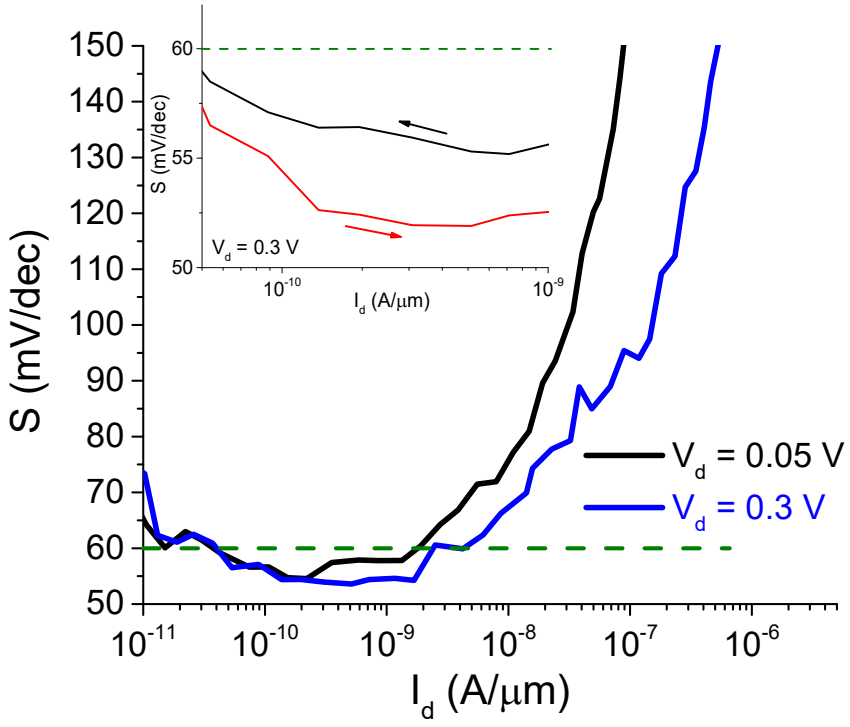


- Saturated output characteristics
- Clear negative differential resistance
- Peak to valley ratio of 3.4 @ V_{gs} = 0.6 V

Zhao, EDL 2017

VNW-TFET subthreshold characteristics





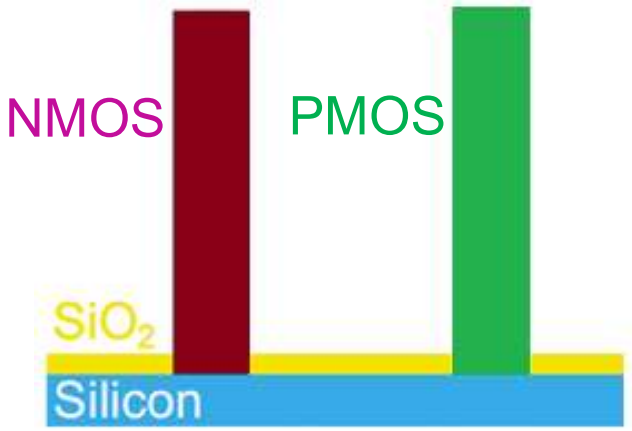
- Sub-thermal for 2 orders of magnitude of current
  - S_{lin} = 55 mV/dec
  - S_{sat} = 53 mV/dec

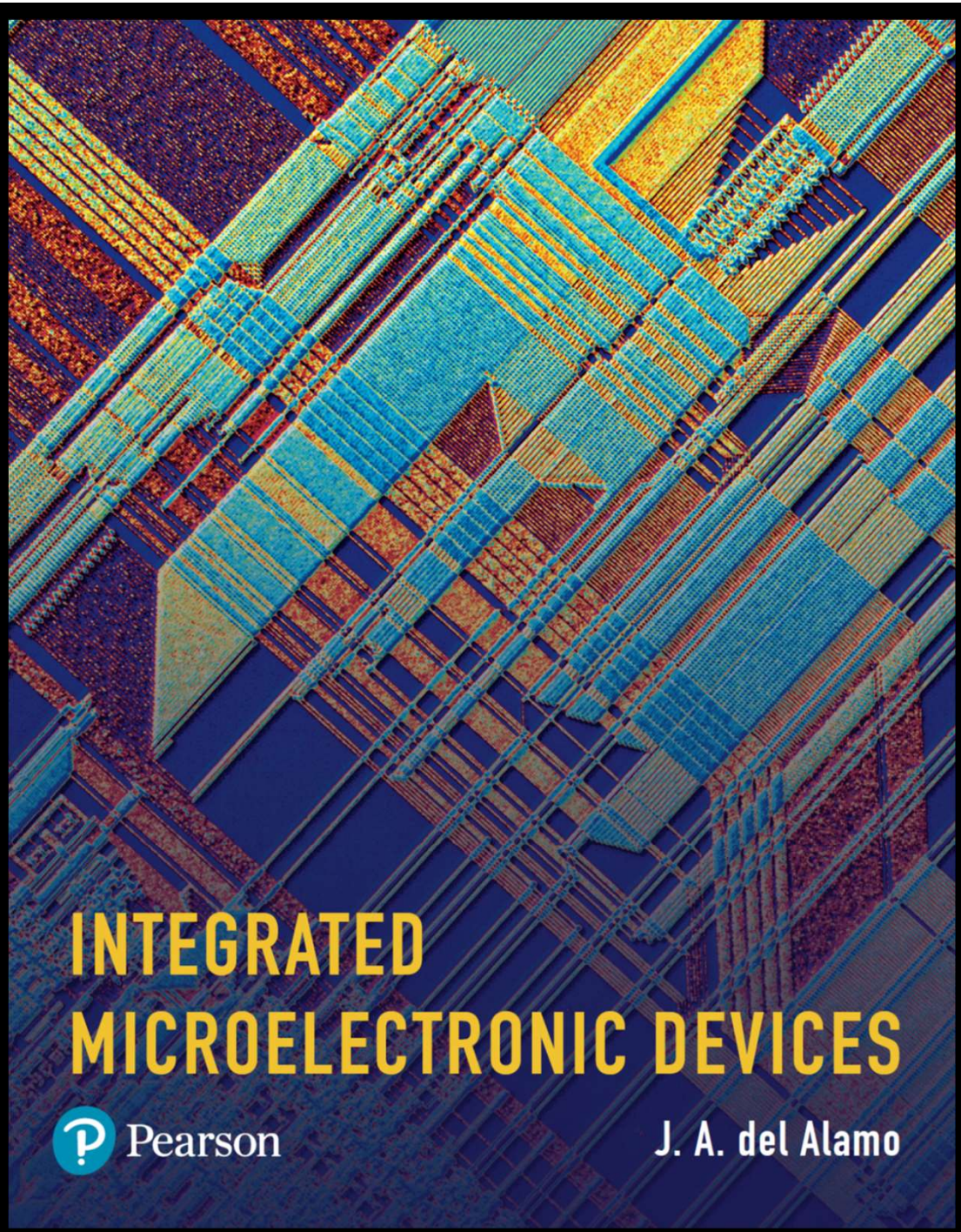
Zhao, EDL 2017

Conclusions

1. Great recent progress on planar, fin and nanowire InGaAs MOSFETs
2. Device performance still lacking for 3D architecture designs

   → severe oxide trapping masks true transistor potential
3. Vertical Nanowire MOSFET: ultimate scalable transistor; integrates well on Si

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